Abstract—This paper presents a low-voltage, low-ripple voltage-controlled charge pump regulator intended to feed internal blocks in a chip to guarantee regular operation when the power supply voltage drops below some predefined value. The circuit was implemented using an array of voltage doubler with system regulation improved by a voltage-controlled oscillator in the feedback path and applying a highly efficient voltage ripple minimization technique. The circuit size is 0.556 mm² when fabricated in a standard 0.25 µm CMOS process and can supply loads consuming up to 8mA from 1.6V to 2.3V of power supply.

Index Terms—Voltage doubler, charge pump, low-ripple, voltage regulator.

I. INTRODUCTION

Nowadays, System On a Chip (SoC) can integrate several functions onto a single die to reduce cost and improve the final product miniaturization. The demand now is for multi-processing units, microcontrollers, graphics, logic, memories (SRAM, Flash, and DRAM), mixed signal, and so on.

Process scaling down and applications requirements are driving SoC devices to operate with low power and low voltage, sometimes down to 1.6V. If one or more internal blocks can not work properly at such low voltage, a higher than the external supply voltage must be generated internally to guarantee the correct operation of the particular module as well as the chip as a whole.

A voltage higher than the power supply level can be generated multiplying that supply voltage. This effect can be achieved connecting coupler capacitors serially through diodes or switches as shown in Fig 1. Basically, for one multiplying stage, the supply voltage is applied to the top capacitor plate during the clock phase \( \phi \) charging it at \( V_{dd} \). Next, in the complementary clock phase \( \phi_b \) the supply voltage is applied to the bottom capacitor plate providing a total charged voltage of \( 2V_{dd} \), disregarding charge loss in the circuit. The supply voltage can be multiplied several times adding more stage cascading capacitors.

An on-chip pump generator based on an improved voltage multiplier technique using the Cockcroft-Walton cell has been developed in [1]. The cell is composed by serial capacitors charged by diodes. Fig. 2 and 3 illustrate the classical multiplier technique and the on-chip implementation, respectively. An alternative voltage doubler topology employing three charge pumps has been proposed in [2]. The main charge pump was implemented with cross-coupled NMOS transistors whereas two additional charge pumps are required to bias a NMOS transmission gate and to level shift a control signal. Fig. 4 shows the basic charge pump cell. The circuit is based on the switch capacitor technique and has been widely employed in most advanced charge pumps. An improved circuit with a seemed topology uses two charge pumps for the doubler [3]. However, its application has disadvantages since one charge pump block is needed to boost the bulk voltage of the output transistor. Additionally, in the second charge pump, the bulk of the output transistor is connected to a floating capacitor resulting in charge losses. Furthermore, careful latch up prevention techniques are required. A solution with no charge losses in the junction, applying the bulk-switching concept and adding only two extra transistors without entailing a second charge pump was proposed in [4].

In this work we present an improved approach using only NMOS transistors without bulk biasing as well as free of charge losses requiring only one extra transistor to bias the gate output transistor. In addition, a voltage-controlled oscillator in the feedback path helps to improve the system regulation. Moreover, a highly efficient minimization ripple technique was applied.

This paper is organized as follows. First, the regulation system design is described in Section 2. Next, in Section 3, the voltage doubler circuit trade-off is presented. The experimental results are shown in Section 4. Finally, Section 5 summarizes the conclusions of this work.
II. CIRCUIT ARCHITECTURE

The proposed charge pump circuit is a voltage regulator intended to provide an internal supply voltage. In this particular case a voltage regulator for an on-chip flash memory is presented. In Fig. 5 C3 is the charge pumping storage capacitance whereas the flash memory is represented by a sink current I0 in parallel with a load capacitance C2. The circuit starts to work whenever the external supply voltage falls below 2.15V. At such condition, the output voltage something in between 2.02V and 2.3V remains steady over a wide range of supply voltages, typically from 1.6V to 2.15V. The charge pump regulator allows for write/read/erase operations on the flash memory even when the power supply reaches 1.6V driving up to 8mA current over a temperature range from -40°C to 135°C.

The charge pump regulator contains three separate blocks: a charge pump, a voltage controlled oscillator (VCO) and a low voltage detector circuit. The module operation is based on a voltage doubler working as a charge pump whose output voltage is linearly either increased or decreased as a function of the oscillator frequency. Four voltage doublers compose the charge pump being each one sequentially enabled to reduce the total output voltage ripple. The numbers of voltage doublers is carefully adjusted allowing to efficiently minimizing the ripple. A delay path is also employed to bias VDD, applied on the cross-coupled transistors M2 and M4. When the input clock signal φ goes high the bottom plate of capacitor C2 and the top plate of the C3 is charged at VDD. Next, when φ goes high, the supply voltage is applied to each second capacitor plates and the charge stored in C2 is transferred to the load by M2. The clock signal φ′″, obtained from a shifter, is applied on M4. The capacitors C2 and C3 are charged to 2 VDD via the cross-coupled transistors M2 and M4.

III. CIRCUIT DESIGN

A. The Charge Pump Voltage Doubler

Employing the same principle presented in Fig. 1 to 4, the voltage doubler implemented with improved serial switch is shown in Fig. 6. In order to achieve a desirable and stable voltage regulation, both the charge pump and the oscillator are designed to compensate each other for supply voltage dependence hence the regulator output voltage is nearly constant across the supply range neglecting process and temperature sensitivities.

Regarding Fig. 6 C2, the voltage doubler capacitor, and C1 are charged to 2VDD via the cross-coupled transistors M2 and M3. When the input clock signal φ goes high the bottom plate of capacitor C1 and the top plate of the C2 is charged at VDD. Next, when φ goes high, the supply voltage is applied to each second capacitor plates and the charge stored in C2 is transferred to the load by M2. The clock signal φ″, obtained from φ′ through an inverter based level shifter, is applied on C3 to obtain a VDD higher than VDD (where Vp is the pump voltage and VDD is the M1 threshold voltage). Note C1 is charged by M4, an extra transistor employed to bias M1 and the capacitor charge is Vp+VDD (~3VDD). The capacitors C1 and C2 can be relatively small as they only drive the gate of M5, M4 and M2, respectively. However, C2 must be carefully adjusted to boost the load with the desirable current.

Assuming the single-phase doubler without load (M1 opened) in Fig. 6 is running freely, i. e. with the control system in open loop, the pump voltage is given by:

\[ V_p = V_{D2} + V_{th3} - V_{DD} \]  

(1)

where \( V_{D2} \) is the drain-source voltage of M2 by the end of the charge process of C2, and \( V_{D2} = (C_2/C_1+C_p) V_p \) is the voltage on C2 due to the capacitive voltage division between C1 and the stray capacitance Cp when \( V_p \) is applied. \( V_p \) is a delayed signal obtained from \( V_p \) with same clock phase. Then, the pump voltage becomes:

\[ V_p = V_{D2} + V_{th3} / (C_1 + C_p) V_p - V_{DD} \]  

(2)
Considering $V_p = V_{dd}$ and $V_{bg2} = 0$, and denoting:

$$\eta = \frac{1}{1 + \frac{C_2}{C_1 + C_p}}, \quad 1 < \eta < 2 \quad (3)$$

the pump voltage due to a single-phase doubler reduces to:

$$V_p \approx \eta V_{dd} \quad (4)$$

Now, after closing $M_1$, the charge pump output voltage needs to be established regarding the charge transference and the ripple voltage. Defining $V_{out}$ as the minimum output voltage, $V_{out}$ as the maximum output voltage, and $f$ as the VCO oscillation frequency, the output ripple voltage is given by:

$$V_{out} - V_{out} = \frac{I_f}{f} \left( C_1 + C_p \right) \quad (5)$$

During the transference period, the charge stored in $C_2$ and $C_p$ is droved out supplying the capacitors $C_2$ and $C_p$. So, the total charge transferred to the output node is:

$$(C_2 + C_p) V_{p} + (C_1 + C_p) V_{out} = (C_1 + C_p) V_{out} \quad (6)$$

If the average value in between $V_{out}$ and $V_{out}$ is $V_{cas}$ replacing (4) and (5) in (6) produces:

$$V_{out} \approx \eta V_{dd} - \frac{I_f}{f} \left[ \frac{1}{C_2 + C_p} + \frac{1}{2(C_1 + C_p)} \right] \quad (7)$$

The term $[1/2(C_2 + C_p)]$ in (7) accounts for the charge previously stored in both $C_2$ and $C_p$, and being sunk by the current load. Note stray capacitances, charge injection, and switching losses might degrade the doubler performance if not taken into account.

Fig. 7 sketches the voltage doubler waveforms in each period of operation with regard to $M_1$ being opened or closed as a function of the clock phases.

Some desirable features obtained in this doubler circuit are the low ripple voltage, small storage capacitor and pump sizes, minimum clock feedthrough, and fast settling time. The ripple voltage minimization is described below. Both the doubler and the pumping storage capacitor sizes must be adjusted as a function of the clock phases and the ripple voltage minimization can be expressed by:

$$C_2 \geq \frac{I_f}{f(V_{out} - \eta V_{dd})} \cdot C_p \quad (8)$$

where $V_{out}$ is the maximum output regulated voltage, e.g. 2.3V in the present case.

It is important to point out the doubler can be implemented with NMOS transistors merely since all gate-to-source voltages are higher than the common-mode voltage ($\sim V_{dd}/2)$ and $V_{bg}$ higher than $\eta V_{dd}$. Also, the layout embodies solid guard rings tied to the ground line and to the pumped output minimizing current injection into the adjacent substrate.

### B. The Minimization Ripple Technique

To attenuate the output voltage ripple a topology with four doublers working sequentially was adopted as mentioned before. The ripple voltage ($V_r$) in open loop can be determined from:

$$V_r \leq \frac{I_{out}}{m f (C_2 + C_p)} \quad (9)$$

where $m$ is the number of doublers. Based in (8-9) the doubler capacitor and the number of doublers were adjusted by simulation to obtain a suitable ripple and meet the overall desired target performance. Fig. 8 illustrates the startup sequence for an architecture with four voltage doublers. The clock signal is delayed evenly in each doubler.

### C. The Voltage Controlled Oscillator

A popular method for realizing digital-output VCOs in CMOS technology is the constant current charge and discharge type or IC oscillator where current sources are used to charge and discharge the timing capacitors and the output frequency is inversely proportional to the capacitor value [5].

Fig. 9 illustrates the voltage controlled oscillator. Assuming the SR latch is in its reset state node $V_{cl}$ is tied to the supply voltage. In this state constant current $I_{on}$ discharges linearly capacitor $C_2$ until the voltage $V_{cl}$ reaches the bandgap voltage $V_{bg}$. Then the output of the comparator controlled by $V_{cl}$ goes high and set the SR latch. After that the discharge of capacitor $C_1$ through current reference $I_{on}$ starts while $V_{cl}$ is quickly tied to $V_{dd}$. When $V_{cl}$ attains the $V_{bg}$ level the circuit is driven to its initial state. This completes one period of oscillation and the process begins again. Note the latch outputs are fed back and their states determine which capacitor is either charged or discharged via the inverter current sources. This method provides a 50% duty cycle square wave.

Assuming $C_2 = C_1 = C$ and $I_{on} = I_{off} = I_{on}$, the voltage controlled oscillator frequency can be approximately given by:

$$f = \frac{1}{2 \pi \sqrt{C \cdot I_{off}}} \quad (10)$$

![Fig. 7. Voltage doubler waveforms](image-url)
Fig. 9. Voltage controlled oscillator architecture

\[ f = 2 \frac{I_{\text{ref}}}{C(V_{dd} - V_{bg})} \]  (10)

Note there is an inversely linear relationship between the supply voltage and the pump-charging rate, the oscillator frequency gets higher as the supply level becomes lower.

To attain temperature and power supply immunity, a temperature compensated voltage and current reference circuits were designed. The bandgap cell supplies a reference voltage that is independent of temperature by canceling the negative temperature coefficient of a bipolar base-emitter voltage \( V_{eb} \) with the positive temperature coefficient of a PTAT circuit (proportional-to-absolute).

The bandgap core in Fig. 9 provides a reference voltage given by:

\[ V_{bg} = V_{bb} + R_2 \frac{m}{n} \ln \left( \frac{R_1}{nR_2} \right) \]  (11)

where \( V_{bb} \) is the base-emitter voltage of transistor \( Q_1 \), \( (m/n) \) is the bipolar emitter ratio, and \( (R_2/R_3) \) is the bandgap resistor ratio.

All the bandgap resistors are implemented with P + diffusion and were adjusted by simulation to meet the required performance.

The current source provides a constant current independent of temperature to discharge the VCO capacitors and bias the comparators. Providing transistors \( M_1 \) and \( M_2 \) work on weak inversion the current reference \( I_{bias2} \) can be defined by:

\[ I_{bias2} = \frac{VR_4}{R_{VRI}} \]  (12)

where \( VR_4 \) is the voltage drop through resistor \( R_4 \) and is given by:

\[ VR_4 = \frac{kT}{q} \ln \left( \frac{W_1}{L_1} \right) \]  (13)

Resistor \( R_4 \) is made up of P + and N-well resistors with complementary temperature dependence carefully adjusted to compensate the PTAT voltage drop in (13).

Considering (10) simultaneously with the charge pump output dependencies on both the oscillator frequency and the power supply voltage as described by (7), the pump regulator has a reasonably constant output voltage disregarding fabrication process and second order effects. However, special care must be taken with comparator offset voltage and capacitor matching. The oscillator switching is very clean and quick wasting very low power consumption with shoot through current sources. An extra design criterion adopted was determining how small the capacitors could be without introducing errors due to stray capacitances in parallel with \( C_1 \) and \( C_2 \).

The voltage controlled oscillator frequency has nearly linear voltage supply dependence and generates nominally a 60MHz square waveform when operating at 1.6V and 22MHz working at 2.1V.

IV. Experimental Results

The charge pump regulator circuit was implemented in a standard 0.25\( \mu \)m CMOS process technology. The regulator occupies an area of 0.212mm\(^2\) whereas the capacitor size is 0.344mm\(^2\).

Fig. 10 exhibits the charge pump regulator performance across the power supply range for 10 parts at room temperature. When the supply falls below 2.3V the charge pump holds its output voltage at about 2.3V. The charge pump regulator output drops off if the power supply becomes lower than 1.6V.

Fig. 11 illustrates the voltage ripple at the regulator output. The nominal ripple voltage at the charge pump output is 70mV pp when driving a load current of 8mA. Moreover, the circuit achieves above 94% power efficiency for a power supply voltage of 1.8V and 8mA current load.
Fig. 11. Output voltage ripple for $V_{dd}=1.8V$ and $I_L=8mA$

Fig. 12. Regulated output voltage across temperature range. Fig. 12 demonstrates the regulator output voltage has a reasonably small variation across a wide temperature range. The regulator transient response after enabling the charge pump is illustrated in Figure 13. With an enable signal falling time of about 50ns, the regulator output voltage stabilizes in less than 600ns. Fig. 14 shows the output regulated voltage for different values of load current.

Fig. 15 shows the VCO frequency as a function of the supply voltage level. Note the oscillator frequency is inversely proportional to the power supply: lower supply voltages cause higher frequencies allowing obtaining a relatively constant voltage at the regulator output.

The microphotograph of the charge pump regulator (four doublers, the VCO and the low voltage detector) including the storage capacitor is shown in Figure 16.

V. CONCLUSION

A voltage-controlled charge pump regulator using NMOS switches with only one extra transistor to bias the output transistor has been developed. Silicon results indicate the circuit has a good load regulation and quite con-
stant output voltage over a wide range of supply voltage and temperature. In addition, a highly efficient minimization ripple technique was presented achieving $70mV_{pp}$ of ripple voltage. The circuit was fabricated in a 0.25µm CMOS technology, and occupies an area of 0.556mm² with a drive capability up to 8mA. The regulator is intended to supply an internal flash memory with constant voltage allowing read/write/erase operations down to 1.6V.

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VII. REFERENCES


