Parameters Extraction from C-V Curves in Triple-Gate FinFET

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ABSTRACT

Methods to determine the effective oxide thickness (EOT), fin height (H_{fin}) and fin doping concentration (N_{fin}) through gate to drain/source capacitance as a function of the front and the back gate voltage curves in triple-gate nMOS FinFET are presented. The proposed methods were validated through three-dimensional numerical simulations and experimental measurements showing that these methods can be also applied in triple-gate nMOS FinFET devices as a powerful tool for experimental validation.

Index Terms: FinFET; CV curve; Electrical Characterization; Effective Oxide Thickness; Fin Height.

1. INTRODUCTION

Miniaturization of MOSFET devices to nanometric dimensions reduced the oxide thickness. This reduction allows a significant tunneling current flowing through the oxide layer. Materials with high dielectric constant (high-\(k\)) have been studied to reduce the tunneling current densities and it was proposed the use of gate stacks with a high-\(k\) dielectric on top of the SiO\(_2\) layer. The poly depletion effect can be avoided changing the polysilicon by TiN gate material. Alternative MOS device architectures have been explored recently. Non-planar multiple gate SOI transistor, as triple-gate FinFETs appears to be one of the most promising structures. The reason is their high immunity to short channel effects and their excellent compatibility with planar CMOS process.

Triple-gate nMOS FinFET structure is presented in Figure 1. TiN is the metal gate, SiO\(_2\) + HfO\(_2\) is the oxide gate stack and the dimensions are EOT as the Effective Oxide Thickness, H_{fin} as the fin height, t_{oxb} as the buried oxide thickness, W_{fin} as the fin width and L as the transistor channel length.

Figure 2a shows the front gate to drain/source capacitances (\(C_{GDS}\)) and Figure 2b represents the two
lateral capacitances ($C_L$) that should be considered in
triple-gate structures (8). If the $W_{fin}$ is large enough,
the triple-gate transistors tend to present a similar
behavior to that of the single gate structures allowing
the neglecting of lateral capacitances.

In this paper we present the application of single
gate SOI MOSFET methods (6) in triple-gate nMOS
FinFETs in order to determine the effective oxide
thickness ($EOT$), fin height ($H_{fin}$) and fin doping con-
centrations ($N_{fin}$). The methods are applied in capaci-
tance-voltage curves (C-V) that are one of the most
commonly used techniques for extracting the MOS-
FET device parameters (7). Three-dimensional numer-
sical simulations and experimental results are used to val-
itate the methods, achieving a good agreement.

2. CV PARAMETER EXTRACTION METHODS

A. Determination of the Effective Oxide
Thickness ($EOT$) and Fin Height ($H_{fin}$)

Figure 3 shows the high frequency $C_{GDS}$ as a
function of $V_{GF}$ for different values of $V_{GB}$. It
can be seen that the $C_{GDS}$ is dependent on $V_{GB}$, which
is affected due to the interaction between front and
back interfaces (10).

When $V_{GF}$ is positive enough, the front inter-
face is inverted and the capacitance $C_{GDS}$ tends to the
front gate oxide capacitance defined as $C_1$. If the front
interface is depleted or accumulated ($V_{GF} < 0.25V$),
the capacitance $C_{GDS}$ depends on the values of $V_{GB}$
due to the coupling between the front and back inter-
faces depletion. Increasing $V_{GB}$ to high positive val-
ues, the back interface is in inversion and the capaci-
tance $C_{GDS}$ tends to be the series association of the
front gate oxide and the fin ($C_{fin}=\frac{\varepsilon \varepsilon_0 W_{fin} L}{H_{fin}}$)
capacitances, defined as $C_2$. On the other hand, for
small value of $V_{GB}$, there is no inversion layer in the
back interface; therefore, $C_{GDS}$ drops to practically
zero, defined as $C_3$ (parasitic capacitance).

$EOT = \frac{C_{ox}}{C_1-C_3}$ \hspace{1cm} (1)

Assuming that $C_2$ is the series association of $C_{ox}$
($C_1$) and $C_{fin}$ capacitance, it is possible to isolate $C_{fin}$
and calculate $H_{fin}$ by equation 2. In this case, the para-
sitic capacitance should be subtracted from $C_1$ and $C_2$.

$H_{fin} = \frac{(C_1-C_3) - (C_2-C_3)}{(C_1-C_3)(C_2-C_3)} W_{fin} L.$ \hspace{1cm} (2)

B. Determination of the Fin Doping
Concentration ($N_{fin}$)

The fin doping concentration ($N_{fin}$) can be
determined interactively through equation 3 with similar
approach used by Nicollian and Brews (7). In this
equation $\phi_{MS1}$ is the metal gate-semiconductor work
function difference, $V_{FB1,inv2}$ is the flat band voltage
with the back interface inverted, $kT/q$ is the thermal
voltage, $n_i$ is the intrinsic concentration of carriers, $q$
is the electron charge and $C_{ox}$ is the front gate capaci-
tance per unit area ($C_{ox}=\frac{\varepsilon_0 EOT}{H_{fin}}$). $EOT$ is previ-
ously calculated by equation 1 and $H_{fin}$ by equation 2.

$N_{fin} = \frac{-\phi_{MS1} \frac{Q_{ox}}{C_{ox}} + \frac{kT}{q} \frac{n_i}{n}_i \left( \frac{C_{fin}}{C_{ox} W_{fin} L} \right) + V_{FB1,inv2} \frac{2C_{ox}}{V_{fin}}}{Q_{ox}}$ \hspace{1cm} (3)

Through the curve of the second derivative of
$C_{GDS}$ in respect to $V_{GB}$ (Figure 4) it is possible to

Figure 3. $C_{GDS}$ vs. $V_{GF}$ curves for several values of $V_{GB}$ in triple-
gate nMOS FinFET.

Figure 4. $C_{GDS}$ as a function of $V_{GB}$ and its second derivative for
a $V_{GF}$ that leaves the first interface accumulated.
obtain the back gate voltage that starts the inversion in the second interface \( (V_{GB,inv2}) \) by measuring the \( V_{GB} \) from the maximum peak. This curve is obtained applying a front gate voltage \( (V_{GF}) \) that leaves the first interface accumulated.

With this back gate voltage \( (V_{GB,inv2}) \) the \( C_{GDS} \) as a function of \( V_{GF} \) curve, presented in Figure 5, is obtained and the \( V_{FB1,inv2} \) can be extracted from the first maximum peak of its second derivative curve.

### C. Simulation results

ATLAS three-dimensional numerical simulations (9) were performed to verify the proposed methods. The triple-gate nMOS FinFETs structures analyzed in this paper were simulated with the following parameters: \( W_{fin}=20 \, \mu m \), \( L=10 \, \mu m \), TiN gate material with work function \( \Phi_M = 4.7 \, eV \), \( EOT=2 \, nm \), \( t_{ox}=145 \, nm \), \( H_{fin}=60 \, nm \), different fin doping concentration, substrate doping concentration \( N_{gb}=1x10^{15} \, cm^{-3} \), LDD extension doping concentration \( N_P=N_S=1x10^{19} \, cm^{-3} \), and with front \( Q_{ox1} \) and back \( Q_{ox2} \) charge oxides negligible.

Simulated \( C_{GDS} \) as a function of \( V_{GF} \) curves are presented in Figure 6 for several values of \( V_{GB} \) and it can be observed the increase of the minimum capacitance for higher \( V_{GB} \) that is a result of second interface inversion.

Figure 7 shows the simulated \( C_{GDS} \) as a function of \( V_{GB} \) curve for \( V_{GF}=-1 \, V \) with the front interface accumulated. The capacitances \( C2 \) and \( C3 \) can be also extracted by this curve. When \( V_{GB} \) is sufficiently high, the back interface is inverted and the capacitance \( C_{GDS} \) is \( C2 \). With negative values of \( V_{GB} \) the back interface is accumulated and the capacitance \( C_{GDS} \) is \( C3 \).

Table I shows the values of \( C1 \), \( C2 \), \( EOT \) and \( H_{fin} \) obtained from the proposed method applied on simulated curves for different values of \( EOT \) and \( H_{fin} \) with \( N_{fin}=2x10^{17} \, cm^{-3} \) and \( V_{GF}=-1.0 \, V \). Results indicate that these methods have a maximum error of 2.0% on \( EOT \) and 7.4% on \( N_{fin} \) for the worst case.

Table II shows \( V_{FB1,inv2} \) obtained from the second derivative of \( C_{GDS} \) in respect to \( V_{GF} \) and \( N_{fin} \) determined by the proposed method for different val-

![Figure 5](image-url)  
**Figure 5.** \( C_{GDS} \) and \( \frac{\delta \, C_{GDS}}{\delta \, V_{GF}} \) vs. \( V_{GF} \) curves for a \( V_{GB,inv2} \) that start the inversion in second interface.

![Figure 6](image-url)  
**Figure 6.** \( C_{GDS} \) vs. \( V_{GF} \) simulated curves for several values of \( V_{GB} \) in triple-gate nMOS FinFET.

![Figure 7](image-url)  
**Figure 7.** \( C_{GDS} \) vs. \( V_{GB} \) simulated curve with \( V_{GF}=-1 \, V \) (front interface accumulated) in triple-gate nMOS FinFET.

### Table I

<table>
<thead>
<tr>
<th>( EOT ) (nm)</th>
<th>( H_{fin} ) (nm)</th>
<th>( C1 ) (pF)</th>
<th>( C2 ) (pF)</th>
<th>( C3 ) (pF)</th>
<th>( EOT ) Error %</th>
<th>( H_{fin} ) Error %</th>
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<td>7.21</td>
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### Table II

<table>
<thead>
<tr>
<th>( N_{fin} ) (cm^{-3})</th>
<th>( V_{FB1,inv2} ) (V)</th>
<th>( EOT ) (nm)</th>
<th>( H_{fin} ) (nm)</th>
<th>( C1 ) (pF)</th>
<th>( C2 ) (pF)</th>
<th>( C3 ) (pF)</th>
<th>( EOT ) Error %</th>
<th>( H_{fin} ) Error %</th>
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<td>1.17x10^{17}</td>
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<td>17.0</td>
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<td>2.03x10^{17}</td>
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<td></td>
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<td>3x10^{17}</td>
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<td>3.30x10^{17}</td>
<td>12.6</td>
<td>10.0</td>
<td></td>
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</table>
ues of $N_{\text{fin}}$ ($H_{\text{fin}}=60\text{nm}$, $\text{EOT}=2\text{nm}$ and $t_{\text{ox}}=145\text{nm}$). Fin doping concentration less than $N_{\text{fin}}=1\times10^{17}\text{ cm}^{-3}$ showed a higher error because the considerations used for $N_{\text{fin}}$ determination (eq. [3]) cannot be used anymore. Another imposition of the method is that it can only be applied to fully depleted structures.

Collaert et al. reported (11) that in multiple gate SOI MOSFETs with fin doping concentration ($N_{\text{fin}}$) less than $2\times10^{17}\text{ cm}^{-3}$ the threshold voltage becomes independent of $N_{\text{fin}}$ exceeding the conventional $2\phi_{F}$ definition of the threshold voltage. Based on this study, the methods were not applied for fin doping concentration ($N_{\text{fin}}$) less than $2\times10^{17}\text{ cm}^{-3}$.

Figure 8 present the $C_{\text{GDS}}$ vs. $V_{\text{GB}}$ curve and its second derivative with $V_{\text{GF}}=-1\text{ V}$ for different fin doping concentrations. When $N_{\text{fin}}$ is increased, a higher back gate voltage ($V_{\text{GB}}$) is necessary to invert the back interface.

The sensitivity of the proposed methods is analyzed in Table III for $H_{\text{fin}}=60\text{nm}$, $W_{\text{fin}}=20\mu\text{m}$, $L=10\mu\text{m}$, $\text{EOT}=2\text{nm}$, $t_{\text{ox}}=145\text{nm}$, $N_{\text{fin}}=2\times10^{17}\text{ cm}^{-3}$, $V_{\text{GF}}=-1\text{V}$ with $Q_{\text{ox1}}=Q_{\text{ox2}}=0$. The maximum error on $\text{EOT}$, $H_{\text{fin}}$, $N_{\text{fin}}$ determination is 5.4, 8.1 and 36.5%, respectively, which are acceptable errors for these parameters in many applications.

In order to analyze the interfaces operation mode, the potential in the middle of the channel was simulated for $V_{\text{GB}}=8\text{ V}$, $N_{\text{fin}}=1\times10^{17}\text{ cm}^{-3}$ and different values of $V_{\text{GF}}$, as shown in Figure 9. It is possible to see that for values of $V_{\text{GF}}$ lower than $V_{\text{GF}}=-1.0\text{ V}$, the front interface is strongly accumulated (front interface surface potential in accumulation $\phi_{\text{SFacc}}$). Simultaneously the back interface is depleted and $C_{\text{GDS}}$ can be considered as $C_{3}$. Increasing the front gate voltage ($V_{\text{GF}}=-0.5\text{ V}$), the front interface starts the “accumulation for depletion transition” (near $V_{\text{FB1,inv2}}$), while the back interface is near the inversion (fin/buried oxide interface surface potential in inversion $\phi_{\text{SBinv}}$), resulting in $C_{\text{GDS}}=C_{2}$. With $V_{\text{GF}}=0.5\text{ V}$ the front and back interfaces are inverted (the surface potential is described as two times level of Fermi $\phi_{\text{F}}$), and no difference can be seen in $C_{\text{GDS}}$ that is tending to $C_{1}$.

**D. Experimental Results**

The proposed methods were verified against experimental measurements of triple-gate FinFETs. They were fabricated starting from SOI nMOSFETs undoped wafers ($N_{\text{fin}}=1\times10^{15}\text{ cm}^{-3}$) with 145 nm buried oxide thickness, following the process described in Ref. (10). The top silicon layer thickness, which is the fin height ($H_{\text{fin}}$), is patterned with 60 nm. After the silicon film definition, a 1 nm thick interfacial thermal oxide is grown, followed by the atomic layer deposition (ALD) of 2 nm HfO$_2$, resulting in an effective oxide thickness of $\text{EOT}=2.0\text{ nm}$. The gate stack is completed with a 5 nm thick TiN ALD film and a 100 nm polysilicon layer. The measured devices have channel length of 10$\mu$m, width of 5, 10 and 20$\mu$m. The high frequency C-V curves were performed with HP4280 LCR Meter at 1 MHz using the HP4140 Picoamperimeter to polarize the substrate ($V_{\text{GB}}$).

Figure 10 present the curves of $C_{\text{GDS}}$ as a function of $V_{\text{GF}}$ for different values of $V_{\text{GB}}$ in a triple-gate FinFET with channel width of $W_{\text{fin}}=20\mu\text{m}$. A level appears in C-V curves, near the depletion region, as the back gate voltage increases. The curve of $C_{\text{GDS}}$ as a function of $V_{\text{GB}}$ curve with $V_{\text{GF}}=-0.5\text{ V}$ (leaving the first interface accumulated) is shown in Figure 11 were the capacitances $C_{2}$ and $C_{3}$ can be seen.

**Table III. Maximum error on EOT, $H_{\text{fin}}$, and $N_{\text{fin}}$ determination as a function of some electrical and process parameter.**

<table>
<thead>
<tr>
<th>Measurements / Parameters</th>
<th>EOT %</th>
<th>$H_{\text{fin}}$ %</th>
<th>$N_{\text{fin}}$ %</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{FB1,inv2}}$ ± 5 %</td>
<td>–</td>
<td>–</td>
<td>96.5</td>
</tr>
<tr>
<td>$V_{\text{GB,inv2}}$ (0.5 V step)</td>
<td>–</td>
<td>–</td>
<td>36.0</td>
</tr>
<tr>
<td>$V_{\text{GF}}$ ± 0.2 nm</td>
<td>–</td>
<td>–</td>
<td>17.7</td>
</tr>
<tr>
<td>$H_{\text{fin}}$ ± 1 nm</td>
<td>–</td>
<td>–</td>
<td>0.5</td>
</tr>
<tr>
<td>$C_{1}$ ± 5%</td>
<td>5.4</td>
<td>&lt;0.5</td>
<td>–</td>
</tr>
<tr>
<td>$C_{2}$ ± 5%</td>
<td>5.4</td>
<td>8.1</td>
<td>–</td>
</tr>
<tr>
<td>$C_{3}$ ± 5%</td>
<td>–</td>
<td>&lt;0.5</td>
<td>–</td>
</tr>
</tbody>
</table>
Table IV present the values of EOT and fin height calculated by the proposed methods, for different channel widths. The maximum error found was 1.99% for the effective oxide thickness and 1.52% for the fin height. The parameters obtained are close to the expected for this technology. Channel width less than 3 µm presented capacitance values very small make difficult its measure, as a conclusion narrow Wfin can be a limitation for the proposed methods.

Unfortunately, the fin doping concentration (Nfin) could not be calculated from the experimental curves because the fin is undoped (Nfin \approx 1 \times 10^{15} \text{ cm}^{-3}) and it is out of range for this method as exposed previously. These methods can also be easily extended to triple-gate pMOS FinFET.

### 3. CONCLUSION

This work presented a technique to determine the effective oxide thickness, fin height and fin doping concentration in triple-gate nMOS FinFET devices. Three-dimensional numerical simulations were used to validate these methods, and good results were achieved. The proposed methods were applied to experimental data, providing coherent results.

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### REFERENCES


