Investigation of the Gate Length and Drain Bias Dependence of the ZTC Biasing Point Instability of N- and P-Channel PD SOI MOSFETs

L. M. Camillo1, J. A. Martino1, E. Simoen2 and C. Claeys2,3
1 LSI/PSI/USP, University of São Paulo, Brazil
2 IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
3 E.E. Dept., KU Leuven, Leuven, Belgium
e-mail: camillo@lsi.usp.br

ABSTRACT

This paper presents an analysis of the instability of the Zero Temperature Coefficient (ZTC) as a function of the gate length and drain bias for partially depleted SOI MOSFETs operating at high temperatures (from room temperature up to 573K). The study takes into account temperature dependent model parameters such as threshold voltage and channel mobility. The analytical predictions are in very close agreement with experimental results in spite of the simplifications used for the V_{ZTC} model as a function of temperature in the linear and the saturation regime.

Index Terms: Zero Temperature Coefficient, temperature dependence, mobility degradation and simple model.

1. INTRODUCTION

High temperature electronics is a large value market that has been difficult to serve up till now. In the automotive field, on-engine and on-transmission applications are projected to require maximum temperatures of up to 200 °C with the wheel-mounted applications going even higher. Further high-temperature application areas include aerospace and environmental monitoring, such as mining and well logging [1].

Several technologies have been explored as a possible choice for high-temperature operation. These technologies include CMOS [2], SOI [3], and GaAs [4]. In MOSFETs, only the top region (0.1-0.2 µm thick) of the silicon wafer is useful for electron transport. Silicon-on-Insulator (SOI) technology is emerging as the most mature solution for high-temperature applications in the MOS technology area. Indeed, SOI MOSFETs present lower leakage currents than bulk devices at high temperature, as well as a smaller variation of threshold voltage with temperature [5]. They are also immune to temperature-induced latchup. As a result, SOI circuits can operate at temperatures above 300 °C, while bulk CMOS is usually limited to 150 °C [6].

For the high-performance applications, partially depleted SOI (PD-SOI) devices are more favorable owing to their better scalability and manufacturability by decoupling the threshold voltage from the silicon film thickness [7]. However, one important issue for the PD-SOI CMOS is the large drop in threshold voltage at high drain biases due to the floating body effect (FBE) [8]. The key to the design of high-temperature analogue CMOS ICs is biasing all circuit stages at ZTC drain currents, which requires that appropriate gate voltages V_{GF} at ZTC (V_{ZTC}) be available on chip. For a given CMOS process, the magnitude of V_{ZTC} is fixed for all n- and p-MOSFETs, and the desired value of the corresponding I_{DS} at ZTC (I_{ZTC}) is obtained by adjusting the W/L ratio [9].

The ZTC is a very important bias point for analog designers as it corresponds to a gate voltage at which the device DC performance remains constant [1], i.e., dI_{DS}(T)/dT = 0. This can be explained as follows. The ZTC gate bias point (V_{ZTC}) is the value of V_{GF} at which the reduction of the threshold voltage is counter-balanced by the reduction of the mobility, and as a result, the value of the drain current remains constant as the temperature varies. For gate voltages lower than V_{ZTC}, the decrease of threshold voltage is dominant and so the drain current increases with temperature, while for gate voltages higher than V_{ZTC}, the mobility degradation predominates and the drain current decreases with temperature. A typical behavior of the drain current (I_{DS}) as a function of front gate voltage (V_{GF}) for the temp-
perature range from 293 K to 423 K is shown in figure 1 and the ZTC point is also indicated.

Some researchers have studied the ZTC point in bulk MOSFETs [9, 10] and partially depleted (PD) SOI devices [11], taking into consideration the temperature dependence of the threshold voltage (Vth) and the mobility (\(\mu_n\)) [9], including the body factor (n) [10] and also the mobility degradation due to the transverse electric field (\(\theta\)) [11].

![Figure 1. Typical IDS x VGF curves for different temperatures in linear and saturation region for a PD SOI device with W/L = 10 µm/10 µm](image)

It is expected that the mutual compensation of the mobility and the threshold voltage temperature dependences may result in a stable ZTC bias point for MOSFETs. However, the mobility compensation is sometimes not enough to satisfy stability in the ZTC point bias [12]. Also, it has been confirmed that ZTC point models should be as simple as possible in order to enable efficient circuit prediction. The goal of this work is to analyse the influence of the gate length and drain bias on the ZTC biasing point in both linear and saturation regions of partially depleted SOI MOSFETs. Experimental results are used to validate the model proposed, using the same approach as reference [13].

2. DEVICE CHARACTERISTICS

The transistor structures used in this work are partially depleted (PD), enhancement-mode n- and p-channel SOI-MOSFETs fabricated using a 0.13 µm SOI CMOS technology at IMEC/Belgium. For these devices, standard UNIBOND material with a 400 nm thick buried oxide was used. The gate stack consists of 2.5 nm Nitride Oxide (NO) and a 150 nm polysilicon gate electrode. The PELOX technique was employed for field isolation and the final silicon film thickness is 100 nm. After the gate definition, low energy ion implantation of arsenic is performed for the formation of shallow source/drain extensions followed by the angled halo implants to control the short-channel characteristics in the nMOSFETs, whereas boron is employed in the pMOSFETs. The halo length is in the order of 65 nm.

3. ZTC ANALYTICAL MODEL

To evaluate the ZTC stability, the V_{GF} value obtained by the cross point between the drain current \(I_{DS}\) versus the gate voltage \(V_{GF}\) curves for two temperatures \(T_1\) and \(T_2\), is defined as \(V_{ZTC_{1,2}}\) as shown in conceptual figure 2.

Therefore, \(V_{ZTC_{1,2}}\) can be calculated as shown in equations (1) for the linear and (2), (3) and (4) for the saturation region [13].

\[
V_{ZTC_{1,2}} \text{(LIN)} = A + nV_{DS}/2 \quad (1)
\]

\[
V_{ZTC_{1,2}} \text{(SAT)} = A + (A^2 - B)^{1/2} \quad (2)
\]

Where

\[
A = (\mu_{n1}V_{th1} - \mu_{n2}V_{th2})/(\mu_{n1}-\mu_{n2}) \quad (3)
\]

\[
B = (\mu_{n1}V_{th1}^2 - \mu_{n2}V_{th2}^2)/(\mu_{n1}-\mu_{n2}) \quad (4)
\]

and \(V_{th}\) is the threshold voltage, \(\mu_n\) is the effective mobility, where the index 1 means that the parameters were obtained in the temperature reference \(T_1 = 300\) K.

Considering that the body factor \(n_1 \approx n_2 \approx n\), the mobility degradation due to the transverse electric field \(\theta_1 \approx \theta_2\) and the temperature dependence of the effective electron mobility is assumed to be given by equation (5), \(V_{ZTC_{1,2}}\) can be calculated based on equations (6) for the linear and (2), (7) and (8) for the saturation region, respectively.

\[
\mu_{n2} = \mu_{n1}(T_1/T_2)^C \quad (5)
\]

\[
V_{ZTC_{1,2}} \text{(LIN)} = A + nV_{DS}/2 \quad (6)
\]

\[
A = V_{th1} + (V_{th1}V_{th2}(T_1/T_2)^C)/(1-(T_1/T_2)^C) \quad (7)
\]

\[
B = ((V_{th1}^2V_{th2}^2)(T_1/T_2)^C)/(1-(T_1/T_2)^C) \quad (8)
\]
The threshold voltage in the linear region was derived by the linear extrapolation method, where the threshold voltage corresponds with the gate voltage axis intercept of the linear extrapolation of the $I_{DS}-V_{GS}$ characteristics at its maximum first derivative (slope) point [14]. In the saturation region the threshold voltage was extracted by the ratio method (RM), which determines the gate voltage axis intercept of the ratio of the drain current to the square root of the transconductance [15]. This model [13] was evaluated to SOI nMOS devices, however this work it is found to pMOS devices and lower channel lengths.

4. RESULTS AND DISCUSSION

In order to verify the influence of the gate length and drain bias on the ZTC biasing point, experimental results from PD-SOI n- and p-MOSFETs with different geometries were obtained. The test devices were measured in the linear ($V_{DS} = 25 \text{ mV}$) and saturation ($V_{DS} = 1.425 \text{ V}$) regions for temperatures between 300 K and 573 K.

Figures 3, 4, 5 and 6 show the $V_{ZTC}$ obtained experimentally and by the simple model [13] for PD SOI nMOS and pMOS devices operating in the linear and saturation region, respectively, for 0.5, 1, 5 and 10 µm channel length. The $V_{ZTC}$ was found by the simple model using equations (6) (linear) and (2, 7, 8) (saturation), and the average value of the $c$ parameter over the temperature range considered was employed.

The data show that for PD SOI nMOS the $V_{ZTC}$ in the saturation region is lower than in the linear region, but on the other hand for PD SOI pMOS presents almost the same level of the $V_{ZTC}$ for both regions. The nMOS devices present the $V_{ZTC}$ in both regions more pronounced at lower channel lengths,
however, the pMOS devices show different trends for the linear and saturation regimes.

Current SOI MOSFET technologies make use of halo or pocket implants [16-18] for improved scaling and control of short-channel effects. These processes result in non-uniform channel doping profiles along the device length, which in turn gives rise to the well known reverse short-channel effect (RSCE) and this effect can be observed in the threshold voltage behavior. As a result the same effect occurs in VZTC, which can be seen as a function of channel length, as shown in figure 7 for PD SOI nMOS in the linear and saturation region and figure 8 for PD SOI pMOS in the linear region. However the effect was not observed in pMOS devices operating in saturation region, shown in figure 9.

At high temperature, lattice scattering degrades the carrier mobility which leads to a reduction of the drain current. When the temperature increases, the intrinsic concentration increases and the Fermi potential decreases [19, 20]. As a result, the depletion charge decreases which causes a threshold voltage reduction with temperature increment.

In figures 10 and 11 one can see the influence of the drain bias (VDS) on the Vth and µn, respectively. The reduction in the threshold voltage (Vth) and channel mobility (µn) with high drain bias leads to a decrease in the VZTC. The reduction in the threshold voltage ∆Vth can be expressed as a function of VDS [21]. The mobility reduction due to the saturation of the carrier velocity in the presence of high longitudinal electric fields (VDS) is modeled by the effective mobility degradation in [22].

The effect of drain voltage on the VZTC is shown in figures 12 and 13 for nMOS and pMOS, respectively.

<table>
<thead>
<tr>
<th>PD-SOI nMOS</th>
<th>W = 10µm Na = 5.5 10^{17} cm^{-3}</th>
<th>t_{oxf} = 2.5 nm t_{oxb} = 390 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>323 → 473</td>
<td>373 → 523</td>
</tr>
<tr>
<td>V ZTC [V]</td>
<td>VDS = -25 mV</td>
<td>VDS = 1.425 mV</td>
</tr>
</tbody>
</table>

Figure 7. V ZTC as function of the channel length obtained experimentally for PD nMOS SOI devices operating in linear and saturation region, having 0.5, 1, 5 and 10 µm channel length.

<table>
<thead>
<tr>
<th>PD-SOI nMOS</th>
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</tbody>
</table>

Figure 8. V ZTC as function of the channel length obtained experimentally for PD pMOS SOI devices operating in linear region, having 0.5, 1, 5 and 10 µm channel length.

Figure 9. V ZTC as function of the channel length obtained experimentally for PD pMOS SOI devices operating in saturation region, having 0.5, 1, 5 and 10 µm channel length.

Figure 10. Experimental threshold voltage (Vth) versus VDS for a PD nMOS OI from 300 K to 573 K
The decrease in the ZTC bias point to higher $V_{DS}$ might be due to the effect of DIBL on the threshold voltage as the potential barrier to form the conduction channel is controlled by both the gate-to-source bias ($V_{GS}$) and the drain-to-source bias ($V_{DS}$). When $V_{DS}$ increases, the potential barrier decreases leading to drain-induced-barrier-lowering (DIBL) causing the threshold voltage to drop \citep{21, 23}. Hence one obtains a lower ZTC bias point at high drain bias for a SOI MOSFET \citep{19}.

The equations 2, 6, 7 and 8 show clearly that when $V_{th1}$ decreases, $V_{ZTC}$ also decreases which is in agreement with the experimental results obtained in figures 12 and 13.

5. CONCLUSIONS

In this paper a simple model is used to study the influence of the drain bias and gate length of partially depleted SOI MOSFETs on the ZTC biasing point in both linear and saturation regions.

The proposed model shows a good agreement between experimental and simulated results both linear and saturation regions.

The $V_{ZTC}$ in the temperature range investigated showed that in the saturation region its value is lower than in the linear region for nMOS devices, and becomes more pronounced at lower channel lengths for both device types. The RSCE effect observed in the threshold voltage behavior can consequently also be noticed when studying $V_{ZTC}$ as a function of channel length for nMOS devices.

The variation of the ZTC bias point with the $V_{DS}$ showed a $V_{ZTC}$ decrease at higher drain bias because of the decreases of the threshold voltage due to the DIBL effect and the impact of the drain bias on the channel mobility.

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