PECVD Silicon Oxynitride as Insulator for MDMO-PPV Thin-Film Transistors

Marco R. Cavallari¹, Katia F. Albertin¹, Gerson dos Santos¹, Carlos A. S. Ramos¹, Inés Pereyra¹, Fernando J. Fonseca¹, and Adnei M. de Andrade²

¹Escola Politécnica da Universidade de São Paulo (EPUSP), Departamento de Engenharia de Sistemas Eletrônicos. Av. Prof. Luciano Gualberto, 158 trav. 3, CEP 05508-970, Butantã, São Paulo, SP, Brazil
²Instituto de Eletrotécnica e Energia da Universidade de São Paulo (IEE-USP). Av. Prof. Luciano Gualberto, 1289 CEP 05508-970, Butantã, São Paulo, SP, Brazil, e-mail: fernando.fonseca@poli.usp.br

1. INTRODUCTION

Flexible displays and sensors in the field of organic or plastic electronics research have experienced dramatic increase in the current decade, involving many academic and industrial research efforts [1]. Conjugated polymers as poly[2-methoxy-5-(3',7'-dimethyloctyloxy)-1,4-phenylenevinylene] (MDMO-PPV) are solution processed and, for this reason, excellent candidates for low-cost and large-area electronics. Particularly due to the emerging necessity of non-conventional energy supply, MDMO-PPV has been extensively studied in solar cells [2], but this polymer can also be used in light-emitting diodes (LED) [3] and transistors for active-matrix organic displays (AMOLED) [4].

Poly(o-methoxy aniline) (POMA) transistors on p-doped silicon substrate presents p-type behavior and hole mobilities of 2x10⁻⁴ cm²/Vs [10]. Polythiophene derivatives exhibit highly-oriented crystals with hole mobilities of 0.2-0.6 cm²/Vs, which are close to those of amorphous hydrogenated silicon TFTs [11].

The main parameters in OTFT characterization are mobility (µ), on-off modulation (ION/OFF), sub-threshold slope (S), threshold voltage (Vₜ) and hysteresis. As newly synthesized materials are released continuously, it becomes clear that charge carrier mobility in those materials probably will become the differentiation factor to classify them [12]. Nonetheless, one must take into account that accuracy in mobility parameter may depend on the structure, utilized solvents and electrodes, oxide-semiconductor interface, low impurity concentration and materials processing [12, 13].

Plasma enhanced chemical vapor deposition (PECVD) technique is considered to be an excellent candidate for fabricating insulator layers due to its low temperature deposition process (≤ 320 °C) and to the easiness of tuning the film dielectric properties with the deposition conditions. SiOₓNᵧ is an alternative of these materials is the strong trapping of electrons [9]. Poly(o-methoxy aniline) (POMA) transistors on p-doped silicon substrate presents p-type behavior and hole mobilities of 2x10⁻⁴ cm²/Vs [10]. Polythiophene derivatives exhibit highly-oriented crystals with hole mobilities of 0.2-0.6 cm²/Vs, which are close to those of amorphous hydrogenated silicon TFTs [11].

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ABSTRACT

We demonstrate that PECVD SiOₓNᵧ with good dielectric properties can replace thermally grown SiO₂ in Organic Thin-Film Transistors (OTFT) applications. It can be used on ITO-covered glass or even flexible substrates. Poly [2-methoxy-S-(3',7'-dimethyloctyloxy)-1,4-phenylenevinylene] (MDMO-PPV) is used as the active layer, due to its wide range of applications such as bulk heterojunction solar cells, light-emitting diodes and light-emitting transistors. We show that charge carrier mobility can be at least two times higher for MDMO-PPV on silicon oxynitride than silicon dioxide, µ₁ 1.1x10⁻⁴ cm²/Vs. MDMO-PPV spun from solvents such as chloroform and toluene provide comparable TFT performance on SiO₂. Preliminary studies of devices with hexamethyldisilazane-treated SiO₂ demonstrate that performance can be further improved by the choice of a proper surface treatment.

Index Terms: organic transistor, MDMO-PPV, hole mobility, SiOₓNᵧ, surface treatment
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dielectric for amorphous silicon thin film transistors technology, whose qualities in metal/oxide/semiconductor (MOS) capacitors have been widely demonstrated [14]. A clear advantage over thermally-grown SiO$_2$ is the possibility to fabricate OTFTs on different substrates, such as indium tin oxide (ITO) covered glass, metal sheets and polymers.

In this context, MDMO-PPV thin-film transistors, utilizing thermally grown SiO$_2$ and PECVD SiO$_x$N$_y$ as gate dielectric layer, were studied. Thermally grown silicon dioxide was utilized for comparative purposes. Insulator properties were controlled by ellipsometry, profilometry and by characterization of MOS capacitors. Whenever it was possible, devices with different insulators shared the same fabrication processes, being this condition essential to enable any comparison, as performance is intrinsically correlated to process parameters. Finally, SiO$_x$N$_y$ was applied on glass-ITO substrates and the resultant TFT performance was then compared to those on Si wafers.

### 2. MATERIAL AND METHODS

OTFTs fabricated were bottom gate bottom contact devices on a 350 µm-thick heavily doped p-type silicon wafer (0.020-0.025 Ω·cm) acting as substrate and common gate electrode. Prior to the insulator deposition, wafers were cut into 1x1 inch$^2$ samples and chemically cleaned by the so-called standard RCA procedure with subsequent etching in diluted HF solution. Silicon dioxide layers were obtained by dry thermal oxidation with 1,1,1-trichloroethane (C$_3$H$_7$Cl$_3$) [15]. Silicon oxynitride without any pre-oxidation and post-annealing treatments was deposited by PECVD with silane (SiH$_4$), nitrous oxide (N$_2$O) and helium (He) precursor gaseous mixtures at 320 °C, 25 mW/cm$^2$ and 120 mTorr. These conditions of deposition were demonstrated to be responsible for a better semiconductor/oxide interface in MOS capacitors, presenting the same thermally grown silicon dioxide quality [14]. Insulator thickness ($x_i$) ranges from 100 to 500 nm. Gold source and drain contacts were 100 nm-thick and were obtained by lift-off after electron beam physical vapor deposition. Channel width/length ($W_{M}$/$L_{M}$) mask values varied from 55 to 220 and $L_{M}$, from 5 to 20 µm. Each sample contained in average 300 transistors. From this ensemble, we randomly chose to characterize 10 OTFTs for each $L_{M}$.

MDMO-PPV (Merck KGaA) in 7 mg/ml chloroform solution was agitated for 24 h, filtered (max. size of 1 µm) and then deposited by spin-coating at 3000 rpm for 60 sec. After deposition, samples were heated at 55 °C and 0.4 mbar during 60 min. The same procedure was applied for MDMO-PPV dissolved in toluene. Resultant average thickness of the films was 100 nm. Organic transistors on glass substrates shared the same processes of TFTs on Si, except for its particular initial cleaning: ITO covered substrates (Delta, unpolished, 30-60 Ω/sq.) were cleaned on ultrasonic bath of acetone (20 min), rinsed with ultra-pure water, immersed on ultrasonic bath of ethyl alcohol (10 min) and dried under nitrogen flow. Device and polymer chemical structure are shown in Figure 1.

Inorganic MOS capacitors on p-type low-doped (100) silicon wafers (1-10 Ω·cm) were prepared from both insulators and used for measuring important parameters such as the dielectric constant and leakage current. More details about their fabrication and characterization are given in [14]. An Alpha Step 100 profilometer and a Rudolph Research Auto E1 ellipsometer (He-Ne laser, 632.8 nm) were used to measure the thickness of the thin-films. Devices were characterized in a HP 4156A parameter analyzer with short integration time and no delay or hold times, being the sample held at room temperature, in darkness and exposed to the atmosphere.

### 3. RESULTS

Table I shows the results for dielectric constant ($\kappa$), effective charge density ($N_{eq}$), density of interface traps ($N_{it}$), leakage current ($J_{leakage}$) and electrical breakdown voltage ($E_{bd}$) obtained from MOS capacitors characterization. $J_{leakage}$ is defined here as the current density flowing through the insulator between the two terminals of our MOS capacitors at 40 V (i.e., at the maximum operating voltage of our OTFTs). Silicon oxynitride capacitors show superior performance with higher $\kappa$ and lower $J_{leakage}$.

Field-effect transistor output characteristics are expressed by drain current ($I_D$) versus drain voltage

<table>
<thead>
<tr>
<th>Insulator</th>
<th>$x_i$ (nm)</th>
<th>$\kappa$</th>
<th>$N_{eq}$ ($10^{10}$ charges/cm$^2$)</th>
<th>$N_{it}$ ($10^{11}$/eV·cm$^2$)</th>
<th>$J_{leakage}$ ($10^6$ A/cm$^2$)</th>
<th>$E_{bd}$ (MV/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>252</td>
<td>3.9</td>
<td>4.7 ± 1.1</td>
<td>1.9</td>
<td>1.6 ± 1.2</td>
<td>9.3 ± 1.3</td>
</tr>
<tr>
<td>SiO$_x$N$_y$</td>
<td>94</td>
<td>4.5</td>
<td>4.9 ± 0.4</td>
<td>1.5</td>
<td>0.15 ± 0.13</td>
<td>3.3 ± 0.3</td>
</tr>
</tbody>
</table>

Table I. Summary of MOS capacitors main parameters for both insulators.
(V_{DS}) for different gate voltages (V_{GS}). Transfer characteristic is given by I_D vs. V_{DS} for different V_{DS}. Typical TFT curves for MDMO-PPV on highly-doped silicon and glass-ITO substrates are shown in Figure 2. Assuming OTFT operation in saturation, i.e. |V_{DS}| > |V_{GS} - V_T|, drain current can be described by the following equation:

\[ I_D = \left( \mu \kappa \varepsilon_0 W/2 \chi L \right) (V_{GS} - V_T)^2 \]  

(1)

where \( \mu \) is the charge carrier mobility, \( \kappa \) is the relative dielectric constant, \( \varepsilon_0 \) is the vacuum dielectric permittivity, \( \chi \) is the insulator thickness, \( W \) is the channel width, \( L \) is the channel length and \( V_T \) is the threshold voltage. Carrier mobility can be extracted from [1] by plotting \( I_D^{1/2} \) vs. \( V_{GS} \) and calculating its first derivative:

\[ \frac{\partial (I_D^{1/2})}{\partial V_{GS}} = \left( \mu \kappa \varepsilon_0 W/2 \chi L \right)^{1/2} \]  

(2)

where the \( V_{GS} \) axis intercept of the tendency curve is equal to the threshold voltage.

Current actually flows through a TFT at voltages below \( V_T \). The \( V_{GS} \) voltage where these first mobile charges are induced in enhancement-type MOSFETs is called the onset voltage \( V_{ON} \). The subthreshold swing can be calculated in the subthreshold region, that is, the regime of operation between \( V_{ON} \) and \( V_T \), considering that \( I_D \) current varies exponentially with \( V_{GS} \). Current modulation is calculated from the relation between the maximum current in on state (\( I_{ON} \)) and in off state (\( I_{OFF} \)). \( V_T \) is calculated only from the off-to-on sweep. All these parameters are illustrated in Figure 3. More details on MOS device parameters are given in [16].

A summary of the main OTFT parameters calculated is shown in Table II. Hole mobilities \( (\mu_h) \) range from 10^{-5} to 10^{-4} cm^2/Vs, threshold voltages \( (V_T) \) were less than 10 V and mostly negative, subthreshold slopes varied from 5 to 10 V/decade, and on/off current modulation between 10^2-10^3. Hysteresis is a bistability in the operational transistor current and appears as a difference in \( I_D \) observed during forward and backward sweeps of \( V_{GS} \). We observe lower back sweep current hysteresis for all devices. Hysteresis factor \( (HF) \) [17] is high for OTFTs on p+-Si/SiOxNy, but comparable to p+-Si/SiO2 for SiOxNy deposited on glass-ITO.

As it will be discussed in Section 4, charge concentration \( (n_Q) \) in the channel must be similar to allow any comparative study on dielectrics for organic transistors. Accumulated charge carrier density is defined as

\[ n_Q = C_i V_{GS}/\varepsilon \]  

(3)
Table III shows that MDMO-PPV spun from toluene TFTs are comparable to devices prepared with chloroform. Although the highest mobility was achieved using toluene on SiOxNy, we will focus on our transistors processed with chloroform solvent. Anyway, these results indicate that high performance on SiOxNy is independent of the polymer solvent.

Higher drain-to-source currents were achieved for shorter channel lengths. Figure 4 shows the \( I_D \) vs. \( V_{DS} \) curve for MDMO-PPV TFT on glass with \( L \sim 1.5 \mu m \). Drain current is higher than 1 µA and \( I_{ON/OFF} > 10^4 \), but saturation region completely disappears.

The effect of changing dielectric thickness on charge carrier mobility is presented in Figure 5. It seems an optimal point exists and is close to 279 nm for SiOxNy and higher than 527 nm for thermal SiO2. Trendlines drawn in Figure 5 give us an idea about the position of these maxima.

As shown in Figure 6, carrier mobility (\( \mu \)) depends also on channel length (\( L \)) and is lower for longer channels (\( L \sim 20 \mu m \)) on p+Si substrates. In Figure 7, one can observe that similar trends were obtained for the subthreshold swing (\( S \)). Increasing channel length also means an increase in \( S \).

The maximum density of traps can be estimated from \( S \) [18] through

\[
N_{\text{trapmax}} = (C_i/\varepsilon) (qS \log e/k_B T - 1) \tag{4}
\]

where \( k_B \) is Boltzmann’s constant, \( T \) is temperature, and \( \varepsilon \) is the base of the natural logarithm. Considering devices on 268 nm-thick SiOxNy, \( N_{\text{trapmax}} \) varies from \((33.2 \pm 9.9) \) to \((5.9 \pm 1.5) \times 10^{12} \) cm\(^{-2} \) when \( L \) changes from 17.5 to 7.3 \( \mu m \). \( N_{\text{trapmax}} \) is

Table II. Summary of the main TFT parameters extracted from \( I_D/V_{GS} \) characteristics for MDMO-PPV dissolved in chloroform and deposited on both insulators and substrates. Channel dimensions are \( W_D = 1.1 \) mm and \( L_D = 5 \) µm.

<table>
<thead>
<tr>
<th>Insulator</th>
<th>( x_i ) (nm)</th>
<th>( n_i ) \times 10^{10} \text{ charges/cm}^2</th>
<th>( \mu_i ) \times 10^{-5} \text{ cm}^2/V s</th>
<th>( V_T ) (V)</th>
<th>( S ) (V/dec.)</th>
<th>( I_{ON/OFF} )</th>
<th>( HF ) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>p+Si SiO2</td>
<td>296 ± 12</td>
<td>2.9 ± 0.1</td>
<td>5.0 ± 0.5</td>
<td>-6.9 ± 3.2</td>
<td>8 ± 1</td>
<td>300</td>
<td>14.4 ± 2.2</td>
</tr>
<tr>
<td>p+Si SiOxNy</td>
<td>279 ± 20</td>
<td>3.6 ± 0.8</td>
<td>11.6 ± 2.6</td>
<td>-8.7 ± 1.0</td>
<td>5 ± 1</td>
<td>1800</td>
<td>22.7 ± 3.5</td>
</tr>
<tr>
<td>ITO/SiOxNy</td>
<td>301 ± 18</td>
<td>3.3 ± 0.2</td>
<td>5.5 ± 2.0</td>
<td>-5.5 ± 0.9</td>
<td>9 ± 1</td>
<td>500</td>
<td>15.4 ± 1.0</td>
</tr>
</tbody>
</table>

Figure 3. Illustration of the method for calculating mobility (\( \mu \)), threshold voltage (\( V_T \)), subthreshold swing (\( S \)) and current modulation (\( I_{ON/OFF} \)). This MDMO-PPV OTFT was fabricated on p+Si/SiOxNy (279 nm).

Figure 4. Absence of saturation for short-channel MDMO-PPV OTFT on ITO/SiOxNy.

(1-1.5) \times 10^{12} \text{ cm}^{-2} \) on 94 nm-thick SiOxNy and decreases from \((8.7 \pm 1.2) \) to \((3.4 \pm 0.6) \times 10^{12} \text{ cm}^{-2} \) when \( L \) goes from 19.8 to 3.9 \( \mu m \) on 527 nm-thick films. Note that in all cases \( N_{\text{trapmax}} \) is higher than \( N_T \) from our conventional MOS capacitors (see Table I).

Let us consider now \( \mu \) dependent on the overdrive voltage (i.e. the difference between \( V_{GS} \) and \( V_T \)) through

\[
\mu = k (V_{GS} - V_T) \tag{5}
\]

where \( k \) contains information on film morphology, being mainly related to the ease of inter-site hopping, and \( \gamma \) is linked to the broadness of an exponential distribution of states (DOS). The Variable-Range Hopping model by Vissenberg and Matters [19] explains this dependence as a consequence of the diminution of the activation energy. According to this model, holes (electrons) move in a distribution of states on the HOMO (LUMO) level and contribute to current flow only when they are excited to a so-called transport energy level. At higher carrier concentration, the average starting energy is closer to the transport energy, which reduces the activation energy and therefore enhances mobility. The drain current in saturation regime (1) becomes:

\[
I_D = k/B (V_{GS} - V_T) \tag{6}
\]

Applying the methodology for parameter extraction from \( I_D \) versus \( V_{GS} \) curves partially exposed above and presented in details in [20], we obtained the results shown in Table IV. The same measurements used for Table II were studied under a varying...
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Table III. Summary of the main TFT parameters extracted from $I_{DS}/V_{GS}$ characteristics for MDMO-PPV dissolved on both solvents and deposited on both insulators. Channel dimensions are $W_T = 1.1 \text{ mm}$ and $L_M = 10 \mu \text{m}$. Charge accumulated is $(3.4 \pm 0.1) \times 10^{14} \text{ cm}^{2} \cdot \text{V}^{-1}$ on SiO$_2$ and $(10.3 \pm 1.4) \times 10^{14} \text{ cm}^{2} \cdot \text{V}^{-1}$ on SiO$_{x}N_y$.

<table>
<thead>
<tr>
<th>Solvent</th>
<th>Insulator</th>
<th>$x_c$ (nm)</th>
<th>$\mu_h (\times 10^3 \text{ cm}^2/\text{Vs})$</th>
<th>$V_T$ (V)</th>
<th>$S$ (V/decade)</th>
<th>$I_{OFF}$</th>
<th>HT (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>chloroform</td>
<td>p+-Si/SiO$_2$</td>
<td>252 ± 10</td>
<td>$2.5 \pm 0.2$</td>
<td>$-5.2 \pm 1.9$</td>
<td>8 ± 1</td>
<td>1500</td>
<td>19.6 ± 3.0</td>
</tr>
<tr>
<td>toluene</td>
<td>p+-Si/SiO$_{x}N_y$</td>
<td>94 ± 12</td>
<td>$3.3 \pm 0.4$</td>
<td>$-21.0 \pm 3.8$</td>
<td>4 ± 1</td>
<td>1590</td>
<td>26.6 ± 5.2</td>
</tr>
</tbody>
</table>

Figure 5. $\mu_h$ vs. SiO$_2$ and SiO$_{x}N_y$ thickness on p+-Si. $W_M = 1.1 \text{ mm}$ and $L_M = 10 \mu \text{m}$.

Figure 6. Variation of $\mu_h$ with channel length for (a) SiO$_2$ and (b) SiO$_{x}N_y$ on p+-Si.

Figure 7. Subthreshold slope vs. channel length for SiO$_2$ and SiO$_{x}N_y$ on p+-Si.

Figure 8. MDMO-PPV TFTs on SiO$_{x}N_y$ with $W_M = 1.1 \text{ mm}$ and $L_M = 10 \mu \text{m}$ in saturation regime ($V_{DS} = -40 \text{ V}$). (a) $I_D$ vs. $V_{GS}$ experimental data for p+-Si/SiO$_{x}N_y$ (279 nm) plotted with fitting for constant $\mu$ (method 1: $\mu_h = 1.28 \times 10^{-4} \text{ cm}^2/\text{Vs}$, $V_T = -8.7 \text{ V}$), and gate voltage-dependent $\mu$ (method 2: $y = 0.83$, $V_T = 0 \text{ V}$, $k = 5.39 \times 10^6 \text{ cm}^2/\text{V}^1 \cdot \text{Vs}$, $\mu_h = 1.14 \times 10^{-4} \text{ cm}^2/\text{Vs}$). (b) Mobility dependence on gate voltage for devices on p+-Si (squares), and ITO (pyramids). TFT parameters from Table IV.

mobility. Mobilities calculated at $V_{DS} = V_{GS} = -40 \text{ V}$ for $L_M = 5 \mu \text{m}$ agree well to the ones presented in Table II, staying in the error interval. Both fitting methods applied in saturation regime are shown together with the experimental data in Figure 8.a. It is clear that varying mobility fits much better for lower voltages ($0 < |V_{GS}| < 20 \text{ V}$). A plot of $\mu_h$ vs. $V_{GS}$ for TFTs on both substrates is shown in Figure 8.b. It demonstrates that hole mobility varies by at least one order of magnitude in the chosen voltage operating range.
et al. have shown that sensors based on P3HT p-TFTs transistors \[24, 25\]. Accumulation-type FETs, Goetz behavior was already demonstrated in MDMO-PPV deviation from the ideal characteristic plots, ambipolar (already shown in Figure 8.b). Another source of the electric field through the transistor channel imply a variation of the effective hole mobility with way, bulk phenomena as Poole-Frenkel effect could centralized within the conjugation length along the backbone of a polymer, being the rate-limiting step of the same performance was not observed for OTFTs on glass and trapped charge concentration seems higher than that on silicon. As this oxide can be obtained at low deposition temperatures with dielectric properties comparable to thermal SiO2, it could also be deposited on a wide range of substrates, including flexible plastic ones. By further reducing its processing temperature, we could also develop top gate devices.

As shown in Figure 2, leakage current through gate and channel in addition to ambipolar behavior seem to be responsible for deviations from the ideal MOSFET characteristics. Commonly present in polymeric TFTs, gate induced leakage currents and drain current offset are discussed in \[21, 22\]. Bonfiglio et al. have shown that differences of one order of magnitude might appear in \(I_D\) between MDMO-PPV transistors with common gate – as in our case – and devices with patterned gate \[23\]. Differently from inorganic monocristalline counterparts, electrical transport in polymeric semiconductors is inherently anisotropic at the molecular scale as charges are delocalized within the conjugation length along the backbone of a polymer, being the rate-limiting step of transport the interchain hopping of charges. In this way, bulk phenomena as Poole-Frenkel effect could imply a variation of the effective hole mobility with the electric field through the transistor channel (already shown in Figure 8.b). Another source of deviation from the ideal characteristic plots, ambipolar behavior was already demonstrated in MDMO-PPV transistors \[24, 25\]. Accumulation-type FETs, Goetz et al. have shown that sensors based on P3HT p-TFTs present a positive threshold voltage of about 5 V. Similarly to the majority of the devices herein, a clearly conducting channel is already present at \(V_{GS} = 0\) V [22]. Nonetheless, our comparative study is valid as we characterize in saturation for operating voltages above –40 V and always use the same device structure and metal electrodes.

4. DISCUSSION

These results show that PECVD SiO\(_{x}N\(_{y}\) insulator can substitute SiO\(_2\) in bottom gate bottom contact organic TFTs and can be used onto ITO-covered glass substrate. As this oxide can be obtained at low deposition temperatures with dielectric properties comparable to thermal SiO\(_2\), it could also be deposited on a wide range of substrates, including flexible plastic ones. By further reducing its processing temperature, we could also develop top gate devices.

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A. Hysteresis

Lower back sweep current hysteresis is very often attributed to charge carrier trapping close to the channel and not mobile ions in the dielectric. It means that higher \(N_Q\) values are expected on the interface polymer/dielectric of our OTFTs compared to the silicon capacitors presented in Table I. As \(H\) is higher than 10 % for almost all transistors presented herein, this is a clear indication that surface treatments could be responsible for further improvements on TFT switching speed. Chua et al. \[26\] verified a 10\(^4\) increase of drain current for F8BT n-OTFTs, when SiO\(_2\) was treated with a self-assembled monolayer (SAM) of octadecyl-trichlorosilane (OTS), responsible for the passivation of defects, impurities and SiOH groups present in silica at the interface.

B. Charge carrier mobility

Hole mobility is at least two times higher for PECVD silicon oxynitride on p-Si substrate than for thermally grown SiO\(_2\), probably due to the higher dielectric constant (\(\kappa = 4.5\)) and charge concentration (\(n_Q\)) in the channel. Yoon et al. \[27\] performed a similar comparative study on bilayer dielectrics calculating \(\mu\) for a specific range of accumulated charge carriers, \((4 \times 10^{12})\) cm\(^2\) V\(^{-1}\) s\(^{-1}\). The importance of this parameter is demonstrated in several charge transport studies for PPV-based materials [2, 4, 28]. They show that current is space charge limited (SCL) and \(\mu\) is not only dependent on \(n_Q\) but also on the electric field and temperature. Accumulated charge is slightly higher for devices on SiO\(_{2}N\(_{y}\), what might explain the better results. Anyway, in spite of the higher \(\kappa\) and \(n_Q\), the same performance was not observed for OTFTs on ITO-glass substrates. One can conclude that the same semiconductor/dielectric interface quality is not achieved on glass and trapped charge concentration seems higher than that on silicon.

Carrier mobility values are similar to those reported in the literature for MDMO-PPV TFTs, being in agreement with results presented by Todescato et al.
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for wet cleaning of SiO₂ without hydrofluoric acid [29], where \( \mu_h = 2.5 \times 10^{-6} \text{ cm}^2/\text{V}s, V_T = -8.7 \text{ V and } I_{\text{ON/OFF}} = 130 \). MDMO-PPV was deposited from a chlorobenzene solution on a bottom gate top contact structure for \( L > 100 \mu \text{m} \). No precise information about the bias for mobility calculation was given. As in this work, their OTFT characteristics showed high hysteresis. Our results for silicon oxynitride as gate insulating are superior to previous results for MDMO-PPV from toluene and chlorobenzene solutions by Geens et al. [9].

C. On-off modulation

The low on-off modulation observed is probably due to leakage current through the insulator and residual carrier concentration in the channel when the device is turned off. The channel resistance can be minimized in principle by pursuing aggressive transistor designs, e.g. by producing large \( W/L \). As one can observe in Figure 4, using reduced channel length, however, can be problematic because of non-ideal electrical behavior arising from short-channel devices [13]. Austin and Chou observed a similar phenomenon for P3HT TFTs with nanometric source and drain contacts obtained by nanoimprint lithography [30]. Saturation begins to fade when channel is shortened from 1000 to 200 nm, and completely vanishes at a length of 70 nm. They blame SCL currents due to the high electric field between source and drain.

Series resistance effects become relatively more important as the channel length goes to the submicron scale, due to lower channel resistance and operation voltages. More important, it can depend on the geometry of the contacts. In the staggered configuration employed by Chua et al. [26], the contact area with the semiconductor is larger and electric field lines favor charge injection [31]. Higher mobilities as \( 5 \times 10^{-4} \text{ cm}^2/\text{V}s \) for MDMO-PPV deposited from mixed xylenes on divinyltetramethylsiloxane-bis(benzocyclobutene) hydroxyl-free insulator. Kayashima et al. obtained \( \mu_h = 3.2 \times 10^{-4} \text{ cm}^2/\text{V}s \) for PPV thin films from a water-soluble precursor polymer by drop casting under high-gravity conditions on p+-Si substrate with OTS-treated SiO₂ [32]. Nevertheless, the authors applied a \( V_{DS} \) of -100V and \( V_{GS} \) as high as -80V.

D. Effects of dielectric thickness and channel length on TFT performance

A solution to increase \( \mu_h \) and \( I_{\text{ON/OFF}} \) is to decrease insulator thickness (\( \chi_x \)). Figure 5 demonstrates that \( \chi_x \) can not be reduced arbitrarily on p+-Si substrates as probably higher tunneling currents are attained and device performance is compromised. Alternatively, according to (3), thicker insulators lead to less charge accumulation in the channel impairing performance. A reduction in \( n_Q \) leads to an increase in the charge transport activation energy and so, a decrease in transport states [19]. This leads to an optimum value for a highest mobility. Obviously, the lower thickness limit is set by the quality of the clean room or the insulator deposition conditions.

As shown in Figure 6, \( \mu_h \) is lower for longer channels on p+-Si substrates, what might be due to a low horizontal electric field (\( E// = V_{DS}/L \)) but also working currents comparable to parasitic ones. A Poole-Frenkel-like behavior is observed for almost all thicknesses and a trendline was drawn for SiO₂Nₓ in Figure 6b. It indicates the presence of traps usually localized at the insulator/semiconductor interface or in grain boundaries of polycrystalline semiconductors [33]. The horizontal electric field is higher for shorter channels, reducing the trap energetic barrier and consequently, trapping time. Less dependence on \( L \) for thinner insulators is probably due to a higher carrier accumulation, filling all traps at high voltages. The low mobility values are probably due to leakage currents affecting calculation accuracy.

As shown in Figure 7, much steeper slopes can be obtained by reducing the channel. The maximum density of traps (\( N_{\text{trapmax}} \)) calculated from \( S \) is acceptable and similar to the interval obtained by Yoon and coworkers for high mobility p-type organic semiconductors such as pentacene and \( \alpha, \alpha \text{-dihexylcarbonyl}- \text{quaterthiophene (DHCO-4T), i.e. (1-10) \times 10^{12} \text{ cm}^2 \) [27]. Taking into account the previous discussion for Figure 6, one can conclude that a decrease in \( S \) with \( L \) is probably due to a Poole-Frenkel-like effect, as the maximum density of traps seems lower for shorter channels. Besides, the trend discussed in Figure 5 is also observed here, as lowest slopes are observed for devices on thickest thermal SiO₂ and nice results are achieved for 279 nm-thick silicon oxynitride. The only exception being 94 nm-thick SiO₂Nₓ as it shows the lowest density of traps, in agreement to its invariance with \( L \) presented in Figure 6b.

E. Carrier mobility dependence on gate voltage

Apparently, the lower performance on ITO is not related to a higher concentration of traps, as \( \gamma \) is lower for devices on glass substrates (see Table IV). Secondly, \( V_T \) calculated from the former model for p-OTFTs is usually more negative if compared to values estimated from more complete models. More important, \( V_T \) must approach zero, otherwise it is an indication of defects occurring at the polymer-oxide interface, arising from charged defects in the oxide or the polymer. Results obtained for different substrates are comparable and close to zero. As already remarked by Shaked et al. in [34], for voltages close to zero, there are three main sources of error: (i) leakage current through the insulator (in our case, less than 1 nA); (ii) residual carrier concentration in the channel when the
device is turned off; and (iii) films composed of two or more phases with different DOS [34].

Figure 8.b shows that biasing the devices at voltages higher than 40 V would attain higher hole mobilities on SiOxNy. For VGS = VT = 0 and consequently lower charge concentration in the channel, a higher similarity with charge transport studies in diode-like structure is observed [4].

F. Dielectric surface treatment

A proper self-assembled monolayer or a polymeric buffer thin film must be applied prior to semiconductor deposition to improve performance at low bias voltage. Todescato et al. demonstrate 1.0x10^-3 cm²/Vs hole mobilities and almost no hysteresis for HMDS and poly(methyl methacrylate) (PMMA) surface treatments [29]. Note that traps are not only due to interface states but also to the intrinsic amorphous morphology of polymeric semiconductors. Better results can be achieved with band-like transport such as in mono- and polycrystalline semiconductors, as hysteresis is also due to majority carrier trapping [35]. In our devices, we believe that the best performance will be achieved for θ > 90º on HMDS-treated SiOxNy.

Surface treatments can be applied also for the production of n-OTFTs, as electron conduction in PPV is strongly reduced by the presence of traps [28, 36]. The choice of the proper material could imply in ambipolar transistors and even high performance n-type OTFTs [24], allowing the fabrication of organic CMOS and inverters. Further increase in current modulation can be achieved by patterning the semiconductor layer for reducing undesired currents through the bulk and insulator [21].

5. CONCLUSION

These results demonstrate that SiOxNy can replace SiO2 in OTFTs and could be used on ITO-covered glass or even flexible plastic substrates, since they can be obtained at low deposition temperatures. Charge carrier mobility was at least two times higher for PECVD silicon oxynitride on p+-Si substrate than for silicon dioxide, probably due to the higher dielectric constant and accumulated charge concentration in the channel. MDMO-PPV deposited from either a chloroform or toluene solution could integrate LEDs for AMOLED displays, but also logic circuits due to the ambipolar behavior of this polymer.

For future studies employing high mobility semiconductors (µ > 0.01 cm²/Vs), contact resistance should be considered by choosing a more adequate model. Degradation of OTFT parameters with time, temperature and electric field requires a careful look. Characteristics of the TFTs used in backplanes must be reliably predictable. Obtaining lower carrier concentrations in the channel but at the same time attaining high currents for controlling a LED can be achieved through a proper surface treatment.

The next step would be gate and semiconductor patterning to reduce undesirable currents tenfold. HMDS-treated SiOxNy might probably increase by one order of magnitude the current modulation, increasing reproducibility and reducing hysteresis to almost zero. That way, we predict that competitive OTFTs on silicon oxynitride could soon be commercialized.

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