On the Variability of the Low-Frequency Noise in UTBOX SOI nMOS-FETs

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\section*{ABSTRACT}

The variability of the low-frequency (LF) noise in n-channel MOSFETs fabricated on an Ultra-Thin Buried Oxide (UTBOX) Silicon-on-Insulator (SOI) substrate has been studied and compared with the variability in the threshold voltage and low-field mobility of the same devices. No correlation has been found between the noise magnitude and the DC parameters, suggesting that the traps responsible for the current fluctuations do not affect the latter. A possible explanation is that the LF noise is dominated by Generation-Recombination (GR) centers in the silicon film, which have less impact on the drain current.

\textbf{Index Terms:} FD SOI nMOSFET; low-frequency noise; generation-recombination noise; noise variability.

\section*{I. INTRODUCTION}

The impact of random dopant fluctuations (RDFs) on the threshold voltage variability of deep submicron transistors has been known for quite some time [1-5]. It is one of the major threats for the operation of Flash and SRAM memory cells in the 22 nm CMOS technology node and below. The origin of RDFs is the fact that for short transistors, only a handful, randomly placed dopant atoms are present in the channel, in spite of the increasing concentrations used to control the Short Channel Effects (SCEs) in bulk planar devices. Considering the statistical nature of the ion implantation process readily explains the device-to-device variation in the number of dopants and the resulting threshold voltage ($V_T$). One elegant way out is to use Fully Depleted (FD) Silicon-on-Insulator (SOI) wafers with a nominally undoped body, eliminating largely RDFs. The combination of a thin-film with an ultra-thin buried oxide (UTBOX) further enhances the control over the SCEs, so that UTBOX devices are promising candidates for sub-22 nm technology nodes. One issue which can contribute to the $V_T$ variability, however, is the variation in the film thickness: it is quoted that 1 nm of film thickness change results in a $V_T$ shift of 25 mV (on the order of the thermal voltage at room temperature) [6].

Another source of dynamic fluctuations, becoming more and more problematic for scaled devices, is the so-called Random Telegraph Noise (RTN), which is associated with the statistical variation in the number of traps in the gate dielectric when scaling the device area [7-9]. This leads to fluctuations in $V_T$ with time and also yields a large device-to-device spread in the low-frequency (LF) noise power spectral density (PSD) [10-12]. It is the aim of the present work to investigate the spatial variation of the LF noise of nMOSFETs fabricated in a UTBOX SOI wafer and to search for a possible correlation with static device parameters like the $V_T$ or the low-field electron mobility in linear operation ($m_n$).

\section*{II. EXPERIMENTAL DETAILS}

The studied n-channel MOSFETs have been fabricated on 300 nm UTBOX SOI wafers, with a nominal film thickness $t_f=20$ nm and a buried oxide thickness $t_{box}=10$ nm. Due to the aggressive oxidation during shallow trench isolation (STI) processing, a re-oxidation of the BOX occurs, resulting in a real BOX thickness of 18 nm and a film thickness of ~14 nm, as derived from cross-sectional Transmission Electron Microscopy (TEM). A 5 nm thermal oxide ($SiO_2$) is grown as gate dielectric. The gate electrode consists of 5 nm plasma enhanced atomic layer deposition (PEALD) TiN capped with 100 nm poly-Si. A cross-section micrograph of a similar 69 nm device with...
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$t_f = 14$ nm is represented in Fig. 1. Standard extension and Highly-Doped Drain (HDD) junctions have been fabricated and a high-dose ground-plane B ion implantation through the BOX was applied.

The noise measurements have been executed on wafer using the BTA hardware controlled by the NoisePro software from ProPlusSolutions. N-channel transistors with a width of $W = 1$ mm and an effective length of 105 nm (mask length 170 nm) have been characterized at room temperature. The back-gate was kept grounded. Measurements were performed in linear operation, applying a drain bias of $V_{DS} = 0.05$ V and stepping the gate bias $V_{GS}$ from weak to strong inversion by increments of 50 mV. In order to assess the variability in a more systematic way, 15 identical devices have been evaluated across the diameter of the wafer. Additional devices chosen randomly across the SOI wafer have been measured as well.

Both $V_T$ and $m_n$ have been derived from the input $I_D$-$V_{GS}$ curves in linear operation, using the Y-function method [13], corresponding with:

$$I_D/g_{m1/2} = (m_nC_{ox}V_{DS}W/L)^{1/2} (V_{GS} - V_T)$$

In Eq. (1), $g_{m}$ is the device transconductance and $C_{ox}$ is the capacitance density ($F/cm^2$) of the gate oxide. The threshold voltage is derived from the intercept of a least-squares linear fit to the Y function, while the low-field electron mobility is calculated from the slope.

III. RESULTS

Typical input $I_D$-$V_{GS}$ characteristics in linear operation of 7 similar nMOSFETs across the diameter of the UTBOX SOI wafer are shown in Fig. 2. Slight variations in the subthreshold slope can be observed. On the other hand, much stronger, orders of magnitude changes can be found in Fig. 3, representing the normalized current noise spectral density ($S_I/I_D^2$) versus the drain current $I_D$ at a frequency $f = 25$ Hz for the same transistors. This illustrates once more the stronger variability of the LF noise Power Spectral Density (PSD) for scaled transistors [10-12], especially in weak inversion. This is normally ascribed to the presence of RTN, corresponding with a single oxide trap [7-9,14-17].

It is well-known that depending on the position of the oxide trap with respect to the discrete dopant atoms in the underlying substrate and with respect to the non-uniform filamentary channel (weak inversion) a strong variation of the relative RTN amplitude ($\Delta I_D/I_D$) can be obtained. This, in turn, gives rise to a strong variation in the PSD of the corresponding Lorentzian spectrum. In order to verify this hypothesis, the detailed spectra of a typical “low noise” and “high noise” device are represented in Fig. 4. While in the first case, predominantly a 1/f-like noise spectrum is found (with some small Lorentzian humps due to Generation-Recombination – GR- noise and a frequency exponent $\gamma$ close to 1), the second type of noise spectra is dominated by an excess Lorentzian, indicating the presence of defect-related GR noise.
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The local variation of the \( V_T \), \( m_n \) and the input-referred noise spectral density \( S_{VG} = S_I / g_m^2 \) at 25 Hz can be more clearly seen in Figs 5 and 6. As can be seen, the device parameters are randomly distributed over the wafer diameter. In addition, the \( V_T \) seems to be well correlated with the low-field effective mobility. On the other hand, there is no clear correlation between the \( S_{VG} \) and the DC parameters. For example, device \#25 corresponds with the highest noise magnitude and also with the highest \( V_T \) and \( m_n \). On the contrary, the second noisiest transistor \#29 corresponds with the lowest \( V_T \) and low \( m_n \).

Combining the data of all UTBOX nMOSFETs studied yields the correlation plots of Figs 7 and 8, representing on the one hand the \( S_{VG} \) at threshold voltage and 25 Hz versus \( V_T \) and \( m_n \) and on the other hand, \( m_n \) versus \( V_T \). No clear trend is observed in Figs 7, while there appears to be a linear correlation between \( m_n \) and \( V_T \) in Fig. 8.

Figure 4. Low-frequency noise spectra around \( V_T \) for a 1 mmx0.105 mm UTBOX nMOSFET exhibiting flicker noise (#30) (a) and excess GR noise (#25) (b) around 25 Hz.

Figure 5. Threshold voltage (a) and corresponding low-field effective mobility (b) in linear operation for a set of 1 mmx105 nm FD UTBOX nMOSFETs across the diameter of the SOI wafer.

Figure 6. Input-referred noise spectral density \( S_{VG} \) in linear operation, at threshold voltage and \( f=25 \) Hz for the same UTBOX nMOSFETs as in Fig. 2 and 3, aligned across the diameter of the SOI wafer.
IV. Discussion

It is clear that the LF noise power spectral density of similar 1 mmx105 nm FD SOI nMOSFETs exhibits a wide device-to-device variation over a UTBOX wafer. This variation appears to be uncorrelated with the variation in the DC parameters. In the past, it has often been noted that there exists a correlation between the 1/f noise magnitude and the low-field mobility for widely different types of MOSFETs [18-22]. These observations can be explained by considering that the front gate oxide traps responsible for the low-frequency current fluctuations by trapping and detrapping, at the same time can cause carrier scattering when they are charged (Coulomb scattering), which gives rise to a reduction of the mobility proportional to the oxide trap density $N_{ox}$. In addition, this Coulomb scattering by charged oxide traps gives rise to the so-called correlated mobility fluctuations, resulting in a quadratic increase of the input-referred noise PSD at higher gate voltages in strong inversion.

The noise spectra of Fig. 4 can help to resolve the issue of the absence of a correlation found here. In the case of the high-noise transistor #25, one can clearly observe that the spectrum at 25 Hz is flat and dominated by so-called Generation-Recombination (GR) noise, caused by defects either in the silicon film or in the front gate oxide. In the latter case, a single RTN can be responsible for the Lorentzian spectrum [14]. The low-noise device #30 in Fig. 4a is characterized by a 1/f spectrum at low frequencies with $\gamma$ close to 1. Note the one decade higher LF noise spectral density caused by the excess GR noise in Fig. 4b compared with Fig. 4a, explaining the wide range of noise values at 25 Hz in Fig. 7. The variability in the LF noise is thus due to the presence of excess GR noise, which is related with randomly distributed, processing-induced defects. At the same time, these defects do not impact the $V_T$ or $m_n$, which may explain the absence of a correlation.

To highlight the variability induced by the excess GR noise, devices corresponding with a 1/f noise dominated spectrum are represented by the blue symbols in Figs 7. While the number of 1/f-like devices is rather small, it is clear that their parameters exhibit a tighter distribution, again demonstrating that the excess GR noise is the root cause of the variability in the PSD and of the absence of a correlation with the static parameters. When only considering the blue symbols, it becomes evident that nMOSFETs with a higher low-field electron mobility exhibit a lower noise as well, in line with previous observations [18-22]. At the same time, the threshold voltage shifts to higher values for a smaller 1/f noise PSD. Since the 1/f noise is given by trapping, this indicates that a smaller $N_{ox}$ corresponds with a higher $V_T$ for the nMOSFETs. In other words,
the traps are positively charged. The variability in the 1/f noise can be ascribed in first instance to the usual variability in the border trap density [10]. The associated correlation with the inverse mobility is related to the Coulomb scattering related with charged traps in the oxide.

Can we tell something more about these defects based on the behavior of the GR noise? From Fig. 4b, one can derive that the Lorentzian plateau and corner frequency of the Lorentzian occurring at the lowest frequencies (~25 Hz) is not markedly dependent on the gate voltage. This strongly suggests that the underlying defects are present in the silicon depletion region [23-27]. This opens the door for GR noise spectroscopy as a function of temperature. However, in the case of UTBOX transistors, the film is fully depleted, so that the analysis proposed in, e.g., Ref. [27] may no longer be applicable. In fact, it has recently been shown that implementing a GR noise model for FD UTBOX SOI nMOSFETs results in both gate voltage dependent and independent with the inverse mobility is related to the traps are positively charged. The variability in the 1/f noise can be ascribed in first instance to the usual variability in the border trap density [10]. The associated correlation with the inverse mobility is related to the Coulomb scattering related with charged traps in the oxide.

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rentzian component to the LF noise spectrum. In this way, a kind of back-gate-induced noise spectroscopy should become possible in UTBOX devices.

V. CONCLUSIONS

It has been shown that the LF noise of UTBOX SOI nMOSFETs exhibits a wide distribution across a wafer, which has been ascribed to the random occurrence of GR centers, mainly in the silicon film and contributing an excess Lorentzian component. The observed noise variability is not correlated with the variability in the DC parameters, like the $V_T$ or $m_n$, emphasizing that the GR centers in the silicon film do not markedly affect the static device parameters.

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