Radiation-tolerant CMOS APS Arrays

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Abstract— CMOS Active Pixel Sensors (APS) arrays are an emerging imaging technology targeted at a wide range of consumer, industrial and scientific applications. APS imaging sensors are displacing traditional CCD-based sensors because of lower cost, greater flexibility and ease of integration with advanced low-power electronics. This is achieved at the expense of lower performance in some imaging characteristics with respect to comparable CCD-based sensors. One area where APS sensors may offer performance that may be unattainable in CCD technology is radiation tolerance. This paper describes the basic principles of APS sensors and the fundamentals of ionizing radiation effects on integrated circuits. The layout techniques that allow the design of radiation-tolerant APS arrays in commercial, low cost, CMOS fabrication processes, in view of the construction of particle detectors for diffraction studies in high-energy physics experiments, are discussed.

Index Terms— Active Pixel Sensors, radiation tolerance, imaging technology, CMOS.

I. INTRODUCTION

The Active Pixel Sensor concept has steadily gained acceptance since its introduction in the early 90’s [1]. This increased use is due to the advantages that this kind of sensor has over the established CCD (Charge Coupled Devices) imaging technology: low cost, compatibility with widely available standard CMOS chip technology, flexibility with respect to operating modes and general ease of integration with other analog/digital chips operating at the low supply voltages common in modern consumer electronics. These advantages are somewhat offset by a degraded response in two parameters that greatly influence the ultimate sensitivity achievable: dark current and quantum efficiency. The best CCDs vastly outperform all APS arrays in these respects, but the costs are also unmatched. This fact relegates state-of-the-art CCDs to the highest demanding scientific, defense and industrial applications.

Most of the discussion around the comparative merits of CCDs and APS arrays is centered on their use for imaging in the infrared and visible spectra. Nonetheless, the use of CCDs extends to the particle radiation domain, notably as X-ray sensors for medical digital imaging equipment. Some high-energy physics (HEP) experiments have also used CCDs, but in this domain they have been displaced by a related solid-state sensor, the silicon strip detector. This kind of detector (and derivatives like the silicon pixel sensor) has become the de facto standard for high precision particle tracking applications in HEP. Interestingly, the continued development of the strip detector led to variants, some of which are recognizable as early forms of APS, both monolithically integrated and hybrid mounted. These are known as pixel detectors in the HEP community.

An alternate independent development in the visible imaging domain led to the introduction of the CMOS Active Pixel Sensor. In this concept, the sensor is an active pixel, realized in standard, or minimally modified, CMOS chip fabrication technology. Each active pixel is individually addressable and contains the sensing element and the first stages of the signal processing electronics. The use of a standard technology allows the realization of the entire ancillary signal processing circuitry together with the sensor array on the same chip (monolithic integration).

In the case of HEP particle detectors the basic requirements imposed on the imaging detectors are rather distinct from those of consumer and industrial applications. It’s of course desirable to have the best possible sensitivity translating to minimal noise (e.g. dark current) and maximum signal (related to quantum efficiency), but other factors also come into play. The read-out rate must be very high while the impinging signal ("image") is present only over a very small part (2% or less) of the total imaging region. The most striking difference is certainly the extended exposure to radiation. Because of their susceptibility to particle radiation, conventional CCDs [2] have been pushed almost totally out of consideration in HEP applications.

Active Pixel Sensors are not per se tolerant to radiation (Rad-Tol) but, in a manner similar to that employed to improve modern integrated circuits [3], they can be made more resilient through carefully selected design choices. The work described in this paper aims to develop a CMOS APS array that can be used as the core imaging sensor for a new particle detector intended for diffraction physics studies in HEP experiments.

The paper is organized as follows: in section II the forms of radiation expected in these environments and the effect of their interaction with the devices and structures present in CMOS integrated circuits are described. The techniques to circumvent the problems caused in these circuits are also discussed. In section III the general architecture of APS arrays is presented. In section IV the design of a Rad-Tol Active Pixel Sensor is detailed. A complete 64x64 APS array in 0.6 μm bulk CMOS technology was developed and fabricated in order to validate the concepts proposed. In section V conclusions are drawn with a dis-
II. IONIZING RADIATION EFFECTS ON INTEGRATED CIRCUITS

Under exposure to particle radiation integrated circuits exhibit a range of malfunctioning behavior, which depend on the kind of particle involved, length of exposure and type of circuit fabrication technology. Some degradation is almost instantaneous, while others depend on the cumulative time of exposure. For the purposes of this paper it is useful to distinguish two forms of radiation, according to the most significant result of the interaction; ionizing and non-ionizing.

Ionizing radiation is generally responsible for cumulative degradation effects, known as total integrated dose effects. Non-ionizing radiation is responsible for both total-dose and near-instantaneous effects. The former are known as single-event effects (SEE). They arise due to the trail of charged carriers created in the path of the traversing particle (the ionized channel). This work does not address SEE damage mechanisms to integrated circuits. In fact, in HEP, particle detection is essentially a concern of producing and collecting as much charge as possible from ionized tracks.

Thus, the discussion is focused on the total-dose effects provoked by the accumulation of localized defects in the integrated circuit material.

Ionizing radiation produces charged carrier pairs more or less uniformly throughout the irradiated circuit. Most carrier pairs generated within conductors promptly recombine and disappear, unless an existing electric field pulls them apart. In this case, a brief current pulse appears while the carriers move through the conductor. Within good conductors both carriers have similar drift velocities giving rise to both electron and hole currents, and no net charge remains. Within insulators the positive carriers are nearly immobile while electrons are able to leave the material unimpeded. The insulator develops thus a net positive charge. This is the most important cumulative effect of ionizing radiation.

Non-ionizing radiation also creates ionization pairs, but in a relatively minor scale. This form of radiation is responsible for the displacement of atoms from their positions within the solid through direct collisions. This is its main cumulative dose effect and is known as displacement damage, and in general takes place throughout the volume of the material (bulk damage effects). The exact mechanism depends on many factors, which will not be further discussed.

In CMOS technology the conducting regions in active devices are generally thin and near the surface of the silicon wafer. Due to this, bulk damage is of lesser concern than surface damage, which is paramount. The integration of modern CMOS electronic circuits rely in two fundamental conditions; the realization of many distinct electronic devices on the same substrate through the planar process, and the electrical isolation of any one device from every other in the same substrate. The latest nanometer CMOS technologies are essentially a push of these two fundamentals towards the limits of silicon processing technology.

Total-dose effects degrade both conditions through a combination of insulting layers trapped positive charge and surface effects. In CMOS technology conducting layers placed above the substrate (where active devices reside) are insulated from it by silicon dioxide (SiO2 - glass) layers. The trapped positive charge exerts a vertical electrical field on the surface of the substrate, attracting electrons to the semiconductor-insulator interface. If enough charge is present the electrons will form a conduction layer as shown in Fig. 1.

In a MOS transistor this is equivalent to a change in the threshold voltage (Vth). NMOS devices would exhibit a reduction of Vth towards zero and PMOS devices an increase away from zero. At extreme levels NMOS become impossible to turn off with voltage levels bounded to the circuit supply levels and PMOS become impossible to turn on. Moreover, in standard CMOS technologies the devices are isolated from each other by reverse-biased p-n junctions, which extend up to the Si-SiO2 interface. Excessive positive charge on the overlying SiO2 may suppress the depletion region of the p-n junction in the vicinity of the surface and allow the conduction layer to extend uninterrupted between previously isolated circuit nodes. This happens all over the Si-SiO2 interface, but it's most acute between the source and drain of the NMOS transistor. There, a physical configuration known as bird's beak is formed, due to the transition from the thick field oxide layer to the thin channel oxide. The proximity of the field oxide increases the electric field applied at the edges of the transistor channel, leading to the early onset of a leakage current path following the bird's beak as shown in Fig. 2a.

If trapped charge increases unabated leakage current paths will develop everywhere, starting under conductive layers used as signal wires in the circuit. One usually refers to it as the reduction of the Vth of the parasitic field oxide MOS (foxfet).

The electrons generated by radiation within the SiO2 may be transported to the Si-SiO2 interface depending on the prevailing circuit voltages. Over long time periods (days to years, depending on temperature) the trapped holes will also undergo the same process. The migration of charge carriers close or across the Si-SiO2 interface creates or activates discrete energy states within the forbidden re-
gion between the valence and conduction band of the semiconductor. These states are called traps. The overall mechanism of trap creation and behavior is complicated and not entirely understood [4]. The end result may be an increase or reduction of the effective charge close to the interface. In the transistor channels this equates to a drift of Vth, and it’s known as an annealing effect. The interface traps are also responsible for a reduction of the mobility of majority carriers, which translates to a loss in transistor gain KPN/KPP. Finally, these traps act as additional generation-recombination centers within the depleted region of the surface p-n junctions. This means that the leakage current of the diodes is raised along their perimeters.

This is a simplified overview of the total-dose effects of ionizing radiation on integrated circuits. An in-depth discussion can be found in the references [5][6][7].

The damage mechanisms described cannot in general be eliminated. One can nonetheless employ several mitigating approaches to reduce their impact on the circuit behavior. These are known as radiation-hardening techniques [5]. They can be applied at the process, layout, circuit or system level. One can develop or select a chip fabrication process, which is inherently immune to or little affected by the underlying phenomena. For example, CMOS SOI processes are asserted as rad-hard due to their immunity to a variety of SEE mechanisms. They are susceptible to total-dose damage, though, and they cost more than mainstream CMOS processes. Alternatively, circuits can be less affected by total-dose mechanisms if certain physical layout and circuit design procedures are followed. The layout techniques aim to forestall the appearance of leakage current paths under the field oxide and between source and drain of NMOS transistors. The conduction layer under the field oxide can only appear where the substrate is p-type silicon, and begins where overlying tracks carry signals in the circuit. These tracks will act as gates of parasitic NMOS known as fxofets. In order to rise further the Vth of the parasitic devices one can layout channel-stop p+ around circuit nodes to be kept isolated. A similar technique, proposed in [8], is to introduce electrostatic shielding (field shields), kept grounded or negatively biased, between the field oxide and the p-substrate. These field shields rest on top of a very thin oxide layer, incapable of accumulating enough trapped charge to invert the p-substrate.

The leakage path between the source and drain of the NMOS transistor appears due to the continuous bird's beak between the two ends. A layout solution is to draw closed-geometry NMOS transistors (*ring* devices), where no such path exists, suppressing the problem (Fig. 2b).

![Fig. 2. Bird's beak leakage (a) cannot occur in ring device (b) with gate enclosing source.](image)

Devices fabricated within the boundaries of the N-type regions do not need any special layout, since parasitic leakage paths cannot form there. The drift of Vth and KPN/KPP in both NMOS and PMOS transistors cannot be counteracted by layout techniques, though. Fortunately, deep submicron and nanometer technologies have extremely thin oxide layers under the gate, and a very high quality Si-SiO2 interface. Because of these two properties the charge creation and transport phenomena are nearly absent. The transistors in the latest CMOS technologies are thus inherently rad-hard with respect to total-dose effects. At circuit level, one can improve the tolerance to radiation by choosing architectures less sensitive to increased leakage currents. One should also avoid topologies that rely on a precise relation between the electrical properties of NMOS and PMOS devices. Thus, one should avoid sampled-data systems in favor of continuous-time ones depending mostly on matching of devices of the same type. Generating and maintaining correct bias voltages and currents internally can also be a difficult task. Since in the present case, most of the circuit architecture is constrained by the structure of the APS array the subject will not be developed further.

At system level one can adopt shielding practices and also provide redundancy, such as cold-sparres. These techniques are beyond the scope of this paper.

### III. PRINCIPLES AND ARCHITECTURE OF APS ARRAYS

There are many practical advantages to a solid state imaging system, such as size, power consumption and robustness. Semiconductor sensors, and first among them silicon ones, can be manufactured at reasonable cost since they can leverage the capital investment of the electronics sector. These factors were already in place in the early days of the
microelectronics revolution, and they led to the invention of the CCD in 1970. Today silicon wafers of the highest quality can be had cheaply, and can be further processed into sensors by fully mature industrial microchip technology. Nearly all solid-state imagers are manufactured in silicon, even though photon conversion is relatively poor in this material. The most demanding applications make use of flip-chip technology with indium bumps to mount a silicon electronics chip on top of a non-silicon sensor array, a costly venue. Silicon imagers must be then carefully designed not to squander precious signal!

The working principle of Si sensors is the following; passing photons have an energy dependent probability of interaction with the material. When an interaction happens charge carrier pairs are created, and under the influence of the thermal agitation of the crystal lattice they mostly recombine. If the silicon is doped (i.e., has excess carriers at equilibrium) and not intrinsic then nearly all pairs recombine and disappear. In intrinsic (only thermal carriers exist) silicon one can avoid this by drawing the carriers apart under the influence of an electric field. A photosensor is a structure where such a field is maintained over intrinsic silicon so as to collect as many as possible charge carriers and convert them to an electric signal. The constraints of the fabrication technology and the desired spectral response define which kind of photosensor is used.

In the CCD concept the photoconversion happens in two stages; firstly the acquisition, where charge is accumulated under each individual sensor, and secondly the readout, where the charge is transferred from one sensor to another until it reaches the edge of the array where it’s converted to an electrical signal. The Active Pixel concept consists of putting the electronics adjacent to every sensor [1]. Each Active Pixel can then be individually accessed. The most frequently encountered APS sensing elements are the photomOS and the photodiode. Our description is focused on the photodiode, the element chosen for our APS array. As shown in Fig. 3 in this type of APS each pixel contains a photodiode, a reset transistor (RST), a source follower M (SF) and a switch to select the pixel (SEL).

The pixel can be operated in integrating or continuous mode. In integrating mode the RST is briefly pulsed to connect the cathode of the photodiode to the positive supply rail and then remain floating. The photon-induced electrons that reach the depletion region of the photodiode will discharge the floating node towards ground. This can be sensed remotely by driving SEL, which will close the switch, and passing a bias current through the SF. The voltage at the output will then follow the potential of the cathode. Every individual pixel can be read out in a non-destructive fashion. It’s useful to note that any leakage current reaching the cathode will adversely impact the stored charge. This is known as dark current. It’s also possible to operate the pixel in continuous mode by leaving RST permanently connected to the supply rail. There’ll be a logarithmic relation between output voltage and photon flux.

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![Diagram](image-url)

Fig. 3. (a) Standard photodiode active pixel and (b) proposed implementation with electronic shutter option.

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The pixels can be assembled into an (i, j) array. The SEL signal drives all i pixels of a given row, in parallel. The j pixels of a column have their out node wired to a common bus. The RST signal may be applied row-wise, individually or globally to the entire array. Many variations on this basic arrangement are possible and can be found in the references [1][3][9].

IV. Radiation Tolerant Active Pixel for Particle Detection

Our objective is to use APS arrays as particle-tracking detectors [11] in diffraction physics studies for HEP. In this domain the particles are much more energetic than visible photons and most of the figure-of-merit parameters commonly used for APS sensors lose meaning. Our study here is oriented towards the constraints of our application, nota-
bly radiation damage concerns.

In this application the APS array must function reliably under continuous exposure to ionizing radiation emitted by the particle beam. These are mostly X-rays, gamma rays and electrons, and total exposure time may reach several years. We analyzed the problem, and a chip containing test structures was designed, fabricated and tested. The results led us to conclude that the transistors of modern submicron process are radiation tolerant to acceptable levels, there remaining the problem of containing the leakage current increase through careful circuit layout.

These encouraging results led to the development of a 64x64 prototype imaging array. The block diagram of the fabricated chip are shown in Fig. 4.

The pixel pitch is 25 μm. Every pixel can be individually read-out by its row (x) and column (y) addresses. The x decoder drives the SEL line for the row, and the y decoder drives the analog multiplexer that allows only one of the column signals to reach the output. Both decoders have dedicated ENABLE inputs. Each pixel contains the photodiode sensor shown schematically in Fig. b. The 6-bit decoders with enable are made up of 3 levels of 2-bit decoders, implemented with 3-input static NAND gates.

The 64-input analog multiplexer is built of 3 levels of 4-input analog multiplexers. At the bottom of each column there's a current sink to bias the selected SF transistor. The RST and TX signals are global to the whole array.

The APS array is meant to be operated in integrating mode. The RST signal is asserted and all photodiodes are reset to one Vth below the supply voltage. Once RST is de-asserted, integration starts. Signal can be read out at any time, in any order. This simple scheme is sufficient for validating our concept. The TX transistor has been added to experiment with a snapshot mode of operation (electronic shutter).

The main issue we address in this prototype is the radiation tolerance of the pixel and of the support circuitry. The layout of one pixel is shown in Fig. 5. The pixel contains only NMOS devices, all laid out as rings, thus totally suppressing any leakage path from source to drain. The transistors are enclosed within a ring of p+ diffusion and a polysilicon over thin oxide strip, which is grounded to function as a field shield. This ringed structure avoids the increased leakage that appears under field oxide at the n+/p-sub border [10]. The photodiode is realized by an n+ diffusion on top of the p-substrate, and it's ringed by the same shielding structure, for the same reasons.

Two rings of field shields and p+ diffusions enclose the whole matrix. In between the two rings there's an N-well, which is positively biased. The field shields and p+ diffusions are supposed to impede the invasion of the p-substrate below. The polarized N-well is meant to trap stray electrons generated by photons traversing the substrate outside the bounds of the imaging array. This structure encloses every circuit block that is part of the analog signal path from the pixel to the output of the chip, such as the analog switches.

The analog multiplexer is shown in Fig. 6. Only NMOS transistors are used, because the range of signal voltages is constrained to one Vth below VDD by the pixel itself. All NMOS are closed-geometry ones. The common output node is laid out with the protection structure over its outside perimeter. Each one of these switchboxes is individually ringed in the same fashion as the whole matrix, and it's totally covered over by unused metal layers to minimize the disturbance from any light entering the detector.

Fig. 4. (a) Rad-tolerant 64x64 APS array architecture and (b) fabricated chip.

Fig. 5. Layout of the hardened active pixel
V. CONCLUSIONS AND FUTURE DEVELOPMENTS

The APS array has been successfully fabricated and appears to be functional. Further testing is in preparation to determine its sensitivity to the expected particle spectrum and its tolerance to radiation. If the results are satisfactory we shall move forward to a larger array and to integration of an ADC and the digital logic needed to implement a panel of detectors. A fully functional APS array for particle tracking with fully digital outputs would be a good candidate for a medical imaging system. Radiation tolerant APS arrays could be useful in safety systems for nuclear power plants and also for space applications.

VI. REFERENCES